

Electronic Design

Ideas for Design

1981 ÷ 1995

Precision rectifier operates from single supply

Cashing in on a programmable operational amplifier's ability to operate accurately with input signals that are close to the negative rail, a simple circuit provides precise, unity-gain, full-wave rectification of ac signals up to ± 3 V in a range of dc to 2 kHz. The circuit operates from one 5-V supply and uses very little power—only 320 μ A of quiescent current.

Although the figure shows the circuit connected for 5-V operation, it performs well on other single supply voltages. Its dynamic range can be readily extended by adding offset voltage trimming.

The OP-22 is a micropower programmable op amp with a low input offset voltage and high open-loop gain. For a positive voltage input, amplifier A_1 drives transistor Q_1 and diode D_2 , making the output voltage equal to the input. The output voltage

swing is below the supply voltage by approximately three times the diode voltage drop; thus the peak output voltage is near +3 V. The output of amplifier A_2 goes to negative saturation—about +0.8 V—and Q_2 is consequently reverse-biased and turned off.

For a negative input voltage, A_1 's output goes into negative saturation and Q_1 is gated off. A_2 serves as a unity-gain inverter, with its gain set by the ratio of R_4/R_2 . Since the output voltage will be equal to the input in magnitude but opposite in polarity, it will also be equal to the absolute value of the input voltage.

The minimum input signal level is limited by the input offset voltages. For the OP-22A/E series, this is 300 μ V maximum. The input bias current is 30 nA maximum when the set current, I_{set} , is equal to 10 μ A. If operation over a wide dynamic range and

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accuracy is needed at low signal levels, the input offset adjustments can be added to A_1 and A_2 .

Quiescent current drain is determined by the set current, which is determined by the value of an external resistor, R_{set} . The relationship of the values is approximately

$$I_{set} = \frac{V_s - 2V_{be}}{R_{set}}$$

The slew rate and bandwidth vary directly with the set current. With a 5-V supply and a base-emitter voltage drop of 0.65 V, the set current will be $3.7V/R_{set}$. Though A_1 operates essentially with unity-gain feedback, A_2 operates with a feedback gain of 0.5, the ratio of $R_2/(R_2 + R_4)$. The closed-loop gain bandwidth is made equal and the frequency response symmetrical by making the set current of A_2 twice that of A_1 .

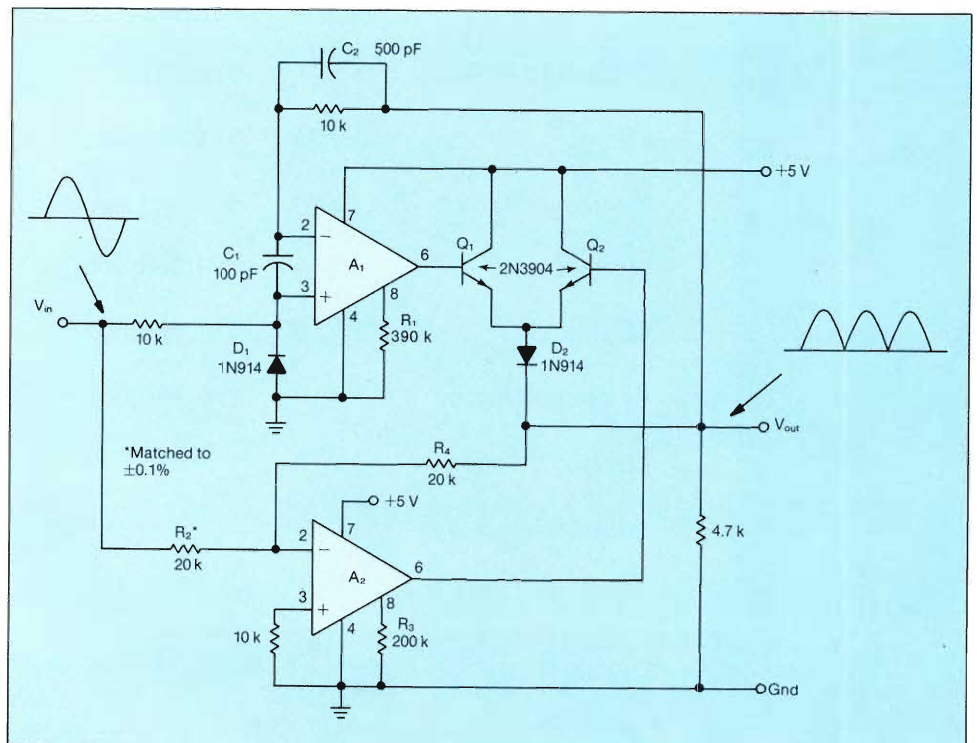
The set current for A_1 is $3.7 V/200 k\Omega$, or $18.5 \mu A$; for A_2 , $3.7 V/390 k\Omega$, or $9.5 \mu A$. These set currents result in quiescent supply currents of approxi-

mately $100 \mu A$ for A_1 and $220 \mu A$ for A_2 .

The op amp's input stage is a pnp Darlington transistor, and a negative input voltage will forward-bias the collector-base junction of the input, pulling the noninverting input of A_1 too negative. To prevent that, a 10-k Ω resistor and a 1N914 diode are added to A_1 's input to limit the input voltage. In addition, if the circuit is operated at higher supply voltages, two diodes—one each in series with the emitters of Q_1 and Q_2 —will protect those transistors. The upper limit of the supply voltage will then be determined only by the op amp's rating, which is +30 V for this circuit.

In addition to its use as a precision rectifier, this circuit is also useful as a precision peak detector provided that a capacitor is placed across the output and the circuit is reset at the end of the detection period.

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Although this precise, full-wave rectifier operates from a single supply voltage, it will accept ac inputs of up to $\pm 3 V$. The operational amplifier's very modest power needs keep quiescent supply drain to just $320 \mu A$.

Design Application

For the trace widths of most electronic printed-circuit board layouts, temperature rise is usually the more realistic design criterion. But power circuits must also consider voltage drop.

Determine PC trace widths with two simple nomograms

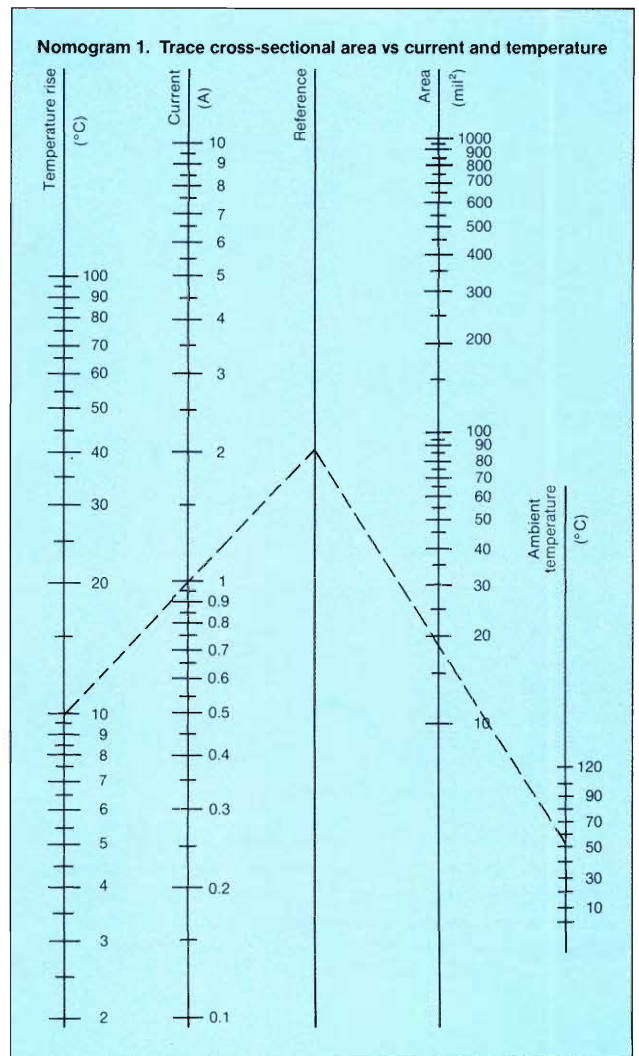
When specifying trace widths for printed-circuit boards, engineers often resort to a rule of thumb based on the traditional values used for power wiring. Two nomograms offer a better approach, however. Not only do they give the correct values simply and quickly—values intended specifically for electronic applications—but also they let the designer visualize the available design options.

The rule-of-thumb method takes the 500 to 1000 circular mils traditionally specified for each ampere of operating current with wire and simply converts the circular area into rectangular area. The appropriate trace width then depends on the weight (thickness) of the PC board's copper cladding and whether plated-through construction is used.

Power-wiring rule unrealistic

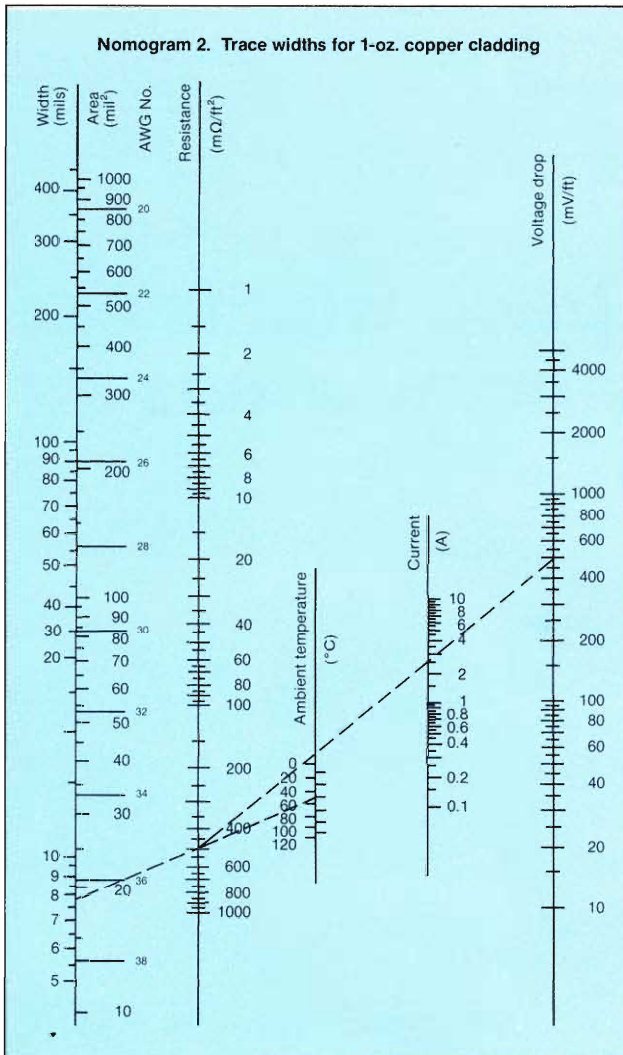
This rule of thumb is a carryover from interior power-wiring specifications established by the National Board of Fire Underwriters (pamphlet 20, section 2202). At 500 circular mils/ampere, the voltage drop is 2% per 100 ft of wire length. Of course, the trace design for printed-circuit boards should be based on more realistic requirements specifically intended for electronic applications, such as MIL-STD-275C and -1495. These standards are based on the allowable temperature rise for PC boards. Accordingly, the factors needed to compute the trace cross-sectional area of a PC board are the maximum ambient temperature, operating current, and the temperature rise normally tolerated by electronic circuits.

These factors can be presented in the form of two nomograms. Nomogram 1 computes the proper



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Determining PC trace widths



trace cross-sectional area, based on the allowed temperature rise for a given current flow and ambient temperature. Nomogram 2 determines the resistance and the resulting voltage drop for the trace cross-sectional area, current flow, and ambient temperature.

In addition, the first scale on nomogram 2 relates the trace area to corresponding AWG sizes. The same scale also shows the widths for traces fabricated with widely used 1-oz copper 2.35 mils thick. But nomogram 2 does not give the optimum trace size, because the relationship between AWG size and trace cross section is based strictly on equal resistance. Instead, nomogram 1 should be used, in power-supply traces where the current is high and small voltage drops can affect the ripple level or supply regulation.

Using the nomograms

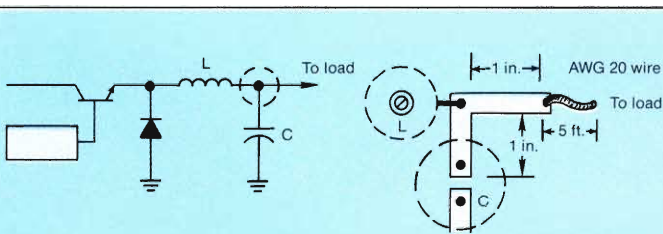
To determine trace cross-sectional area with nomogram 1, draw a line from the desired temperature rise through the operating current to intersect the reference line. Next, draw a line connecting the point of intersection on the reference line with the maximum expected ambient temperature. The required cross-sectional area in square mils is the point of intersection of the line with the area scale. For a 10°C rise with 1 A at 50°C ambient (the example on the nomogram), the area needed is 18 mil², or 7.9 mils wide for 1-oz copper.

To use nomogram 2, draw a line connecting the cross-sectional area and the ambient temperature. The resistance is read at the line intersection on the resistance scale (490 mΩ/ft). The voltage drop is found by drawing a line from the resistance through the current to intersect the voltage-drop scale (490 mV/ft).

A switched-mode power supply is an excellent example of circuitry that must carry heavy currents on PC board traces. To find the proper trace width, first assume a maximum ambient temperature of 75°C and an allowable temperature rise of 40°C. The traces to be specified will connect an inductor to an output capacitor and the latter to the output load (Fig. 2). The traces must carry 5 A to a TTL load. The load is placed 5 ft from the supply, and the load and ground-return and the supply are connected with AWG-20 wires.

Temperature controls

On nomogram 1, align a straight edge along 40°C on the temperature rise scale with 5 A on the current scale and mark the intersection point on the reference line. Rotate the straight edge and line up the point on the reference line with 75°C on line



The traces on a PC board connecting a switching-mode power supply's inductor with the output-filter capacitor and the output carry relatively heavy current, providing a good application of the trace-width nomograms.

ambient temperature scale, then read 85 mil² on the area scale.

To ensure that the benefits from selecting a filter capacitor with a low equivalent series resistance are not negated, now use nomogram 2. Whether remote sensing is incorporated in the power supply or not, the voltage drop along the traces and the connecting wires must be accounted for to ensure proper operation. To calculate the resistance of the trace, draw a line from the cross-sectional area of 85 mil² to an ambient temperature of 75°C. The resistance is 120 mΩ/ft; therefore, for a 1-in. trace length (see figure) the resistance will be 10 mΩ. Although 10 mΩ is a reasonable value, it is still the same order of magnitude as the ESR of a high-quality capacitor; therefore it will be responsible for at least 15 mV of ripple voltage.

Now, with nomogram 2, determine the voltage drop along the trace from the inductor to the output. Draw a line from 120 mΩ/ft on the resistance scale through 5 A on the current scale and read 600 mV/ft on the voltage-drop scale. It can be seen that a 1-in. length will generate a 50-mV voltage drop.

Computing voltage drop

To compute the voltage drop along the two wires (power and ground-return) connecting the supply with the load, use nomogram 2 again. This time draw a line connecting AWG 20 on the area scale to 75°C on the ambient temperature scale and read a resistance of 12 mΩ/ft. Rotate the straight edge and draw a line connecting 12 mΩ/ft on the resistance scale with 5 A on the current scale; read 60 mV/ft of voltage drop. Thus the voltage drop due to the 10 ft of wiring (or 5 ft of cable) will be 600 mV.

In general, the most commonly used temperature rise is 40°C; therefore the temperature scales provided should cover most normal situations. However, if the nomograms do not cover the range of currents required, the scales can be extended by decades by keeping the same lengths per decade. Just reproduce the nomogram, then cut and glue or tape the reproduced scale to the scale to be extended, and renumber the graduations appropriately to correspond with the extended decades. □

Bibliography

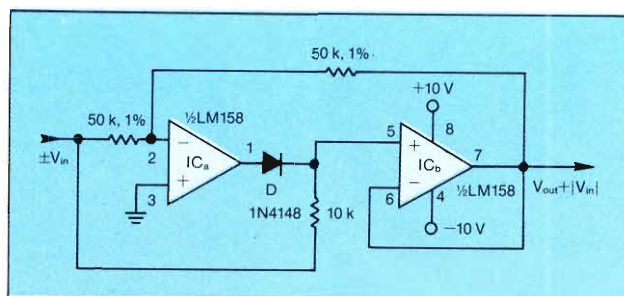
Varney, D. L., "Choose Proper Wire Sizes Quickly with a Programmed TI 59/58," *ELECTRONIC DESIGN*, July 19, 1979, pp. 102-105.

How useful?	Circle
Immediate design application	544
Within the next year	545
Not applicable	546

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Simple circuit yields absolute value

As attractive as a reduced parts count is to a designer, improved performance is even more desirable. The absolute-value circuit shown accomplishes its task with just five parts, three fewer than conventional designs, and represents its output as a positive voltage rather than the negative expression of previous designs. Since some of the eliminated parts are precision resistors, the circuit can do more for less.



The absolute value of an input voltage is always represented by a positive voltage in this simple dual op-amp circuit. Another benefit of this design is the low parts count.

When an input voltage is positive, the output of IC_a is negative and diode D does not conduct; hence the output of IC_b is positive. On the other hand, when the input is negative, the output of IC_a is positive and D will conduct, causing the absolute value, expressed as a positive voltage, to appear on the noninverting input of IC_b and on the circuit's output.

The circuit's dynamic range extends from zero to the point at which the operational amplifier saturates. The bandwidth is determined by the characteristics of the diode and the high-frequency performance of the op amp.

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MOSFET switch driver maintains transformer-coupled pulse waveform

Despite its advantages as an impedance matcher; a step-up, step-down device; and a dc isolator, the secondary winding of a transformer cannot faithfully represent an input pulse train whose duty cycle varies widely from 50%. When used as a low-impedance intermediate stage in a power switch, a MOSFET overcomes the 50% limitation. The circuit in Fig. 1 provides a low-impedance during switching intervals and retains a duty cycle of 1% to 99%.

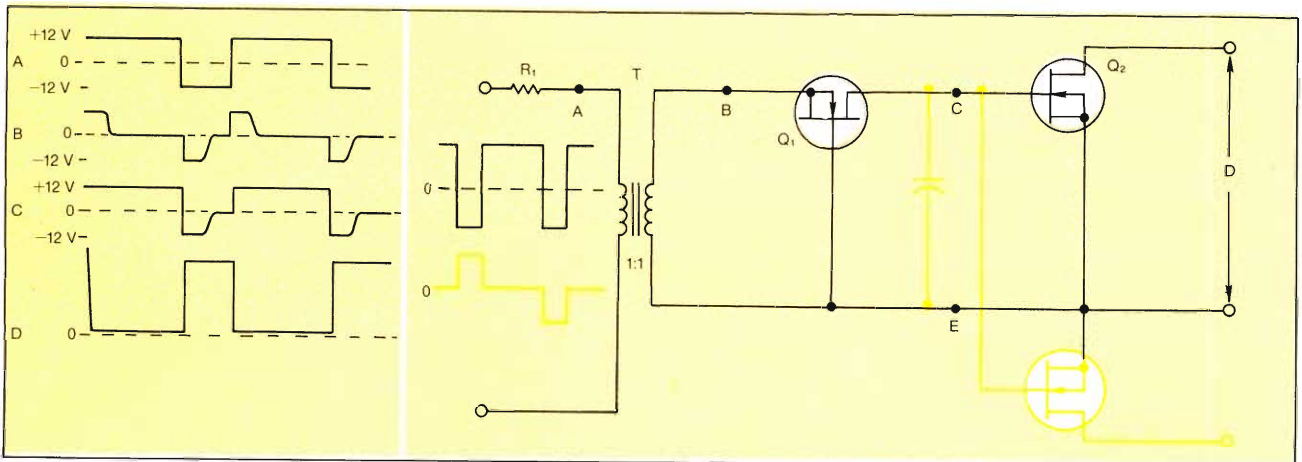
The 50% limit comes about because, in order to maintain the transformer's constant volts-seconds property, the area under its output voltage-vs-time curve must be equal on the positive and negative half cycles. Thus for a positive output of nominal amplitude and pulse width, a large voltage swing is required if a narrow negative pulse must reset the transformer's core flux each cycle. The maximum duty cycle that can be handled by most practical semiconductor circuits is roughly 50% because of the drive-voltage limitations of the semiconductors. The solution is the MOSFET driver.

In the timing diagram, when a logic-level signal

(waveform A) is applied to the primary of transformer T, the output at the secondary (waveform B) is derived from the core flux as it attempts to follow the input until saturation occurs. At this point, the winding's voltage falls to zero and remains there until the core flux is reversed by the negative-going portion of A. Saturation occurs again if the pulse's amplitude-time product exceeds the voltage-vs-time capability of the core.

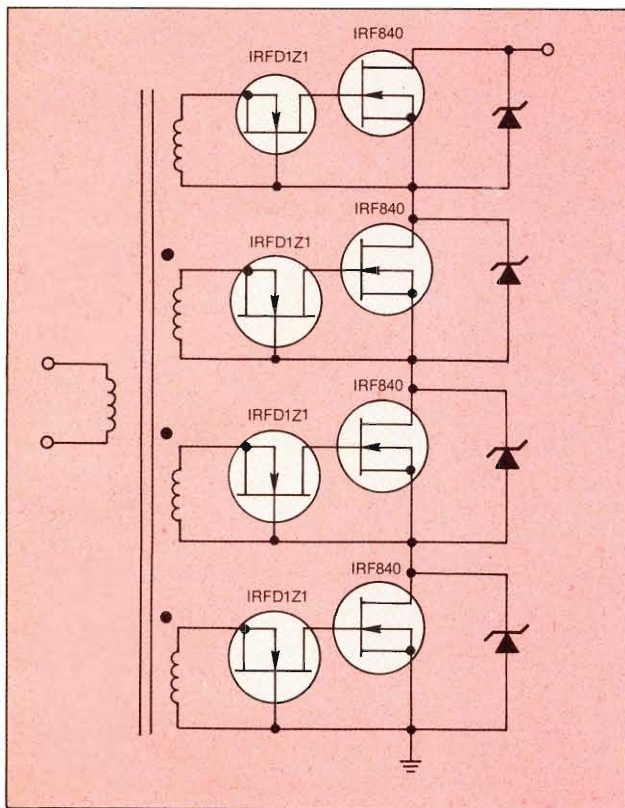
During the positive portion of the cycle, the intrinsic diode of transistor Q_1 is in forward conduction; thus power switch Q_2 is driven on (waveforms C and D). The driving impedance of Q_1 is equal to R_1 plus its intrinsic diode resistance. In a practical circuit, this value can be less than $10\ \Omega$. Thus the turn-on time of Q_2 is about 75 ns. When T saturates, Q_1 isolates the voltage collapse at the secondary winding from the gate of Q_2 . The input capacitance of the switch, C_{iss} , maintains the gate bias for a time limited only by its gate leakage current.

As the input waveform goes toward $-12\ \text{V}$, Q_1 becomes fully enhanced and Q_2 is turned off. The

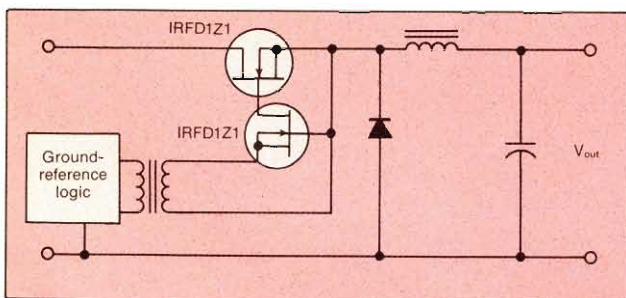


1. By virtue of their low on-state impedance, MOSFET drivers retain the integrity of pulse-width shapes from transformer-coupled circuits. Unipolar and bipolar switches illustrate two examples.

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2. By the use of a multitapped secondary, several devices can be linked via a series-aiding connection to render a switch capable of handling 600 V at 8 A per section.



3. A single-switch regulator that has its own ground-reference logic can be easily built with two MOSFETs.

source impedance of Q_1 at this time is equivalent to $R_1 + R_{ds}(Q_2)$. This value is again less than 10Ω and yields a turn-off time for Q_2 of less than 100 ns.

When T again saturates during the negative half cycle, its winding voltages fall to zero and Q_1 turns off. Transistor Q_2 remains on, however, as Q_1 again provides momentary isolation. The drain voltage at Q_2 will thus be a faithful representation of the input signal, independent of its duty cycle. Power switch Q_2 can be used in many applications that require isolation between low-level logic and a high-power output point.

Several variations of the basic circuit equip it for a myriad of applications. For instance, an ac switch can be created by adding an n-channel power MOSFET as shown in the tinted portion of Fig. 1. The on-off times of such a switch can be extended from seconds to hours by the addition of an external gate-to-source capacitor, C.

For greater noise immunity, a second driver can be added to the circuit of Fig. 1. The added device's drain would be connected to Q_2 's source and its source connected to Q_1 's gate. The device's gate would be connected to Q_1 's drain (Q_2 's gate). Thus when T saturates on its negative swing, the gate of Q_2 remains at the maximum negative bias level until the next positive-going drive pulse.

In Fig. 2, a high-voltage, high-power switch can be configured from a multitapped transformer and several basic MOSFET driver circuits (IRFD 1Z1) joined by a series-aiding connection (IRF840s). A simple single-switch power supply regulator (Fig. 3) can also be constructed using the principles of the MOSFET driver.

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Digital signal-processing technique results in more useful frequency and impulse response measurements from dual-channel FFT analyzers.

Hilbert transform improves FFT analyzer range

The Type 2032 and 2034 dual-channel FFT analyzers use Hilbert transforms to help compute the envelope of signals, making it easy to find peaks, as well as improving the dynamic range of time-domain displays. The instruments, from Denmark's Bruel & Kjaer, lend their digital signal-processing skills to fast measurements of the frequency and impulse responses of low-frequency systems.

The Hilbert transform rotates each frequency component 90° . Thus the Hilbert transform of a cosine results in a sine. Squaring and adding the two functions produces the envelope of the original signal. The benefit of this type of signal detection is that for a sine wave, the envelope produced will be ripple-free.

Unlike signals displayed on conventional oscilloscopes as linear amplitude scales, data computed by the Hilbert transform is displayed on a logarithmic scale, greatly enhancing the usable dynamic range of the signal. In addition, all time-domain functions analyzed by the 2032 or 2034 are complex; that is, they have both real and imaginary parts. This applies to raw time signals, impulse responses, cross-correlation functions, autocorrelation functions, and the cepstrum. It is therefore possible to display not only the envelope of these signals, but also their time domain phase, the slope of which is related to the instantaneous frequency of the signal.

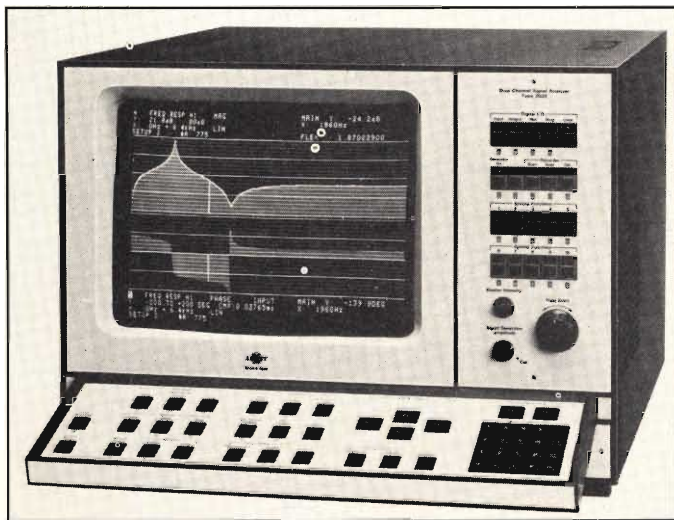
The 2032 and 2034 each contain two 16-bit computer systems us-

ing bit-slice technology for high speed. The first processor is dedicated to signal-processing programs, such as FFTs, averaging, inverse FFTs, and Hilbert transforms. It also handles all triggering under software control. A fast 16-by-16-bit hardware multiplier in the 2032 helps quicken the pace of FFT and averaging operations.

The second processor manages all display tasks, as well as user-interfacing, cursors, and calibration. It drives a bit-mapped raster-scan display with four intensity levels. Special hardware is included for high-speed generation of scale lines and cursors. Also connected to this processor is 6 kbytes of CMOS memory, with battery backup, for storing up to 20 user-defined measurement and display setups.

Other features of the two analyzers include a digital zoom that is implemented using high-speed digital filtering. A total of 14 different digital low-pass filters are fitted to each of the analyzers' two channels, giving a wide choice of frequency spans that can be placed anywhere in the instruments' 1.56-Hz-to-25.6-kHz range.

Bruel & Kjaer, 18, Naerum Hovedgade, 2850 Naerum, Denmark; (45,2) 80 05 00; Telex: 37316 bruka dk.



CIRCLE 502

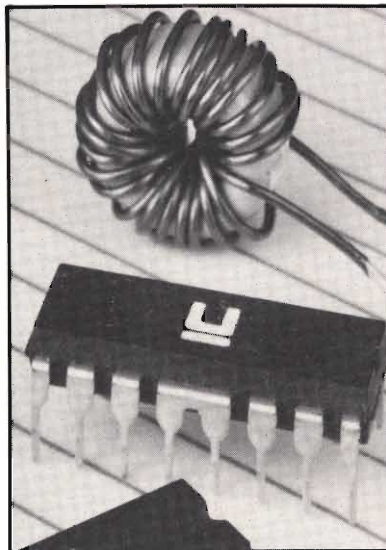
Low-cost controller chip oversees magnetic amps

Magnetic amplifiers regulate multiple power-supply outputs without the wasted energy associated with linear pass regulators. The approach, though, requires more parts and means designing a controller, thereby increasing cost and complexity. Unitrode's UC1838 controller is helping on the latter two fronts by consolidating the needed circuitry onto a \$2.00 chip.

Just one IC houses three previously separate components, a pnp reset current driver, two high-gain op amps, and a precise voltage reference. In addition to the magnetic amplifier, designers need only supply three diodes, output LC filtering, and a few nonprecision resistors.

The UC1838 regulates dc output voltages from 5 to 40 V. The controller samples this voltage through an external divider network, feeding it to the inverting input of one of the op amps. The op amp then serves as an error amplifier, comparing the sample to an internal 2.5-V reference. No external reference is needed, and the op amp's 120 dB of available gain guarantees that the resistors are not heavily loaded.

An output from the error amplifier turns on the base of the pnp driver. In proportion to the magnitude of the error signal, the collector current forces a voltage opposite to the normal polarity across the magnetic core. This controlling current can source whatever amount it takes to saturate the core, up to 100 mA, but should be limited by a series resistor.



The maximum regulated output voltage is 40 V, limited only by the characteristics of the pnp transistor. A 5-V minimum also derived from the auxiliary supply serves as the input to the 2.5-V regulator.

The second op amp can be employed in various ways. It can handle current-limiting or over-voltage shutdown. Alternatively, it may be cascaded with the first op amp, in that way supplying even greater feedback loop gain.

The UC1838, in a ceramic DIP, operates from -55° to $+125^{\circ}$ C. Two other versions, the UC2838 and UC3838, are housed in plastic bat-wing DIPs and work from -25° to $+85^{\circ}$ C and 0° to 70° C. In hundreds, the controllers cost \$5.11, \$3.80, and \$2.00 in order of decreasing thermal capabilities.

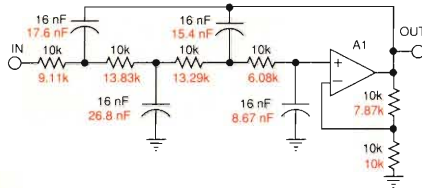
Unitrode Integrated Circuits Corp., 7 Continental Blvd., Merrimack, NH 03054; Joe Pappalardo, (603) 424-2410.

Pamela J. Waterman

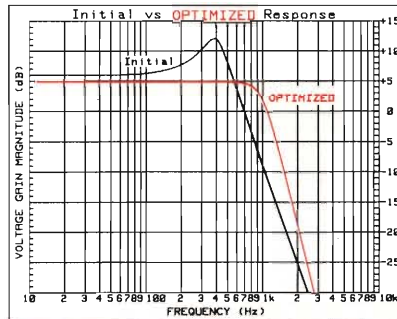
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More Corrections To This Design Idea

Several of your readers have correctly pointed out a significant weakness in my "Universal Off-Line Power Supply Uses Few Components" Idea for Design article published on Dec. 17, 1999 (p. 114). The key issue is the lack of a 100- Ω 1/2-W resistor, which should be placed in series with D1.

Without this resistor, there is a small but finite possibility of destroying D1 during startup. Also, the voltage rating of C1 should be increased to 450 V.

I didn't get any feedback regarding the C1 rating, possibly because the figure shows 120 V ac, and C1 rated at 250 V is more than sufficient. However, the text mentions "Universal" and "maximum of 240 V ac." So the C1 rating should be increased to 450 V.

*Sam Ochi
IXYS Corp.*

ANALOG OUTLOOK

Exploring the world of analog, mixed-signal, and power developments

Learn The Limitations Of Low-Pass Sallen-Key Filters

*Imperfect Amplifiers, Parasitic Capacitance, And Component Selection
All Impact Filter Performance At High Frequencies.*

JIM KARKI, Texas Instruments Inc., 8505 Forest Ln., Dallas, TX 75243

Since professors R.P. Sallen and E.L. Key described it in 1955, the Sallen-Key low-pass filter has become one of the most widely used filters in electronic systems. Perhaps because the mathematics can be somewhat daunting, however, little has been written to help working engineers specify the correct components to achieve their objectives. For example, few realize the limitations of Sallen-Key filters at high frequencies.

The following describes the basic operations of a Sallen-Key low-pass filter and offers a simplified way of working with such circuits. Based on laboratory research, it also demonstrates some of this filter's limitations at high frequencies.

Sallen-Key basics: The two-stage RC network shown in Figure 1 forms a second-order low-pass filter. This circuit has the limitation that its Q is always less than one-half. With $R1 = R2$ and $C1 = C2$, then $Q = 1/3$. Q approaches the maximum value of one-half when the impedance of the second RC is much larger than the first. But most filters usually require larger Q s than one-half.

Q can be enhanced with an amplifier in positive feedback. With that feedback localized to the filter's cutoff frequency, almost any Q can be realized. Mostly, it's only limited by the physical constraints of the power supply and component tolerances. The Sallen-Key low-pass filter shown in Figure 2 is an example of how an amplifier is used in this manner. $C2$ is no longer connected to ground, but

rather provides a positive feedback path around the amplifier.

The operation can be described qualitatively. At low frequencies, where $C1$ and $C2$ appear as open circuits, the signal is simply amplified to the output. $R3$ and $R4$ are chosen to give the desired gain. At high frequencies, $C1$ and $C2$ appear as short circuits, and the signal is shunted to ground at the amplifier's input. The amplifier amplifies this input to its output, and the signal doesn't appear at V_O . Near the cutoff frequency, where the impedance of $C1$ and $C2$ are on the same order as $R1$ and $R2$, positive feedback via $C2$ provides Q enhancement of the signal.

Ideal operation: The standard frequency-domain equation for a second-order low-pass filter is:

$$H_{LP} = \frac{K}{-\left(\frac{f}{f_c}\right)^2 + \frac{jf}{Qf_c} + 1} \quad (1)$$

where f_c is the corner frequency and Q is the quality factor.

When $f \ll f_c$, Equation 1 reduces to

$H_{LP} = K$, and the circuit passes signals multiplied by gain factor K . When $f = f_c$, Equation 1 reduces to: $H_{LP} = -jKQ$, and the signals are enhanced by the factor Q . When $f \gg f_c$, Equation 1 reduces to:

$$H_{LP} = -K\left(\frac{f_c}{f}\right)^2$$

and the signals are attenuated by the square of the frequency ratio. With attenuation at higher frequencies increasing by a power of two, the formula describes a second-order low-pass filter.

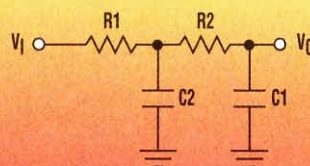
Deriving the transfer function of the circuit in Figure 2, the Sallen-Key ideal low-pass transfer function is defined by Equation 2 (see p. 100).

By letting

$$s = j2\pi f, f_c = \frac{1}{2\pi\sqrt{R1R2C1C2}}, \text{ and}$$

$$Q = \frac{\sqrt{R1R2C1C2}}{R1C1 + R2C1 + R1C2(1-K)},$$

Equation 2 follows the same form as Equation 1. With simplifications, you



$$\frac{V_O}{V_I} = \frac{1}{s^2(R1C2R2C1) + s(R1C2 + R2C1 + R1C1) + 1}$$

1. This two-stage RC network forms a second-order low-pass filter with a maximum Q that's always less than one half. The equation defines the transfer function.

can deal with the equation more easily.

Simplification 1: Set filter components as ratios. Letting $R1 = mR$, $R2 = R$, $C1 = C$, and $C2 = nC$, results in:

$$f_c = \frac{1}{2\pi RC\sqrt{mn}}, \text{ and}$$

$$Q = \frac{\sqrt{mn}}{m+1+mn(1-K)}$$

This simplifies things somewhat, but there's interaction between f_c and Q .

The design should start by setting the gain and Q based on m , n , and K , and then selecting C and calculating R to set f_c . It may be observed that $K = 1 + [(m+1)/(mn)]$ results in $Q = \infty$. With larger values, Q becomes negative. In other words, the poles move into the right half of the s -plane and the circuit oscillates. The most frequently designed filters require low Q values, so this should rarely be a design issue.

Simplification 2: Set filter components as ratios and gain = 1. Letting $R1 = mR$, $R2 = R$, $C1 = C$, $C2 = nC$, and $K = 1$ results in:

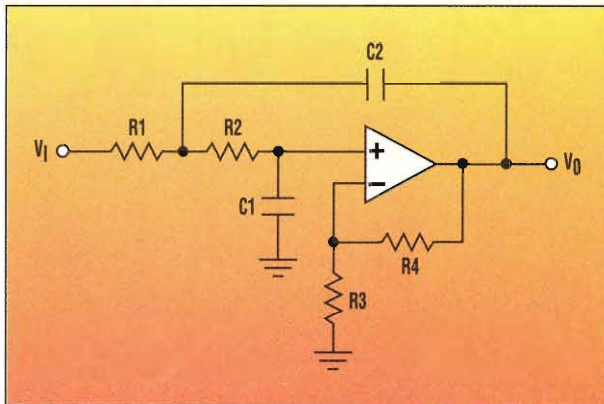
$$f_c = \frac{1}{2\pi RC\sqrt{mn}} \text{ and } Q = \frac{\sqrt{mn}}{m+1}$$

This keeps the gain equal to 1 in the pass band. But again, there's interaction between f_c and Q . Design should start by choosing the ratios m and n to set Q , and then selecting C and calculating R to set f_c .

Simplification 3: Set resistors as ratios and capacitors equal. Letting $R1 = mR$, $R2 = R$, and $C1 = C2 = C$, results in:

$$f_c = \frac{1}{2\pi RC\sqrt{m}} \text{ and } Q = \frac{\sqrt{m}}{1+2m-mK}$$

The main motivation behind setting the capacitors equal is the limited selection of values in comparison with



2. The basic low-pass Sallen-Key filter can be analyzed for three basic modes of operation: below cutoff, in the area of cutoff, and above cutoff. At high frequencies, C1 and C2 act as short circuits, shunting the input signal to ground.

resistors. Interaction exists between setting f_c and Q . Design should start with choosing m and K to set the gain and Q of the circuit before choosing C and calculating R to set f_c .

Simplification 4: Set filter components equal. Letting $R1 = R2 = R$ and $C1 = C2 = C$ results in:

$$f_c = \frac{1}{2\pi RC} \text{ and } Q = \frac{1}{3-K}$$

Now f_c and Q are independent of one another. Design is greatly simplified, although it's simultaneously limited. Q is now determined by the gain of the circuit. The choice of RC sets f_c . The capacitor should be chosen, and the resistor calculated. One minor drawback is that because the gain controls the Q of the circuit, further gain or attenuation may be necessary to achieve the desired signal gain in the passband.

Values of K that are very close to 3 result in high Q s that are sensitive to variations in the component values of $R3$ and $R4$. Setting $K = 2.9$ results in a

nominal Q of 10. A worst-case analysis with 1% resistors results in $Q = 16$. In contrast, if setting $K = 2$ for a Q of 1, worst-case analysis with the same 1% resistors results in $Q = 1.02$. Resistor values where $K = 3$ leads to $Q = \infty$. And with larger values, Q becomes negative. The poles move into the right half of the s -plane and the circuit will oscillate. The most frequently designed filters require

low Q values, so this should rarely become a design issue.

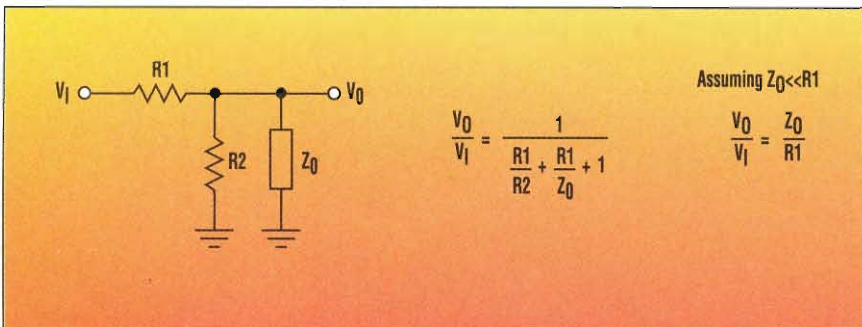
Non-ideal circuit operation: Up to now, we've assumed that the circuit was ideal, but there comes a time (or actually a frequency) when this is no longer valid. Simple logic tells us that the amplifier must be an active component at the frequencies of interest or else we have problems. But what are these problems?

As mentioned previously, there are three basic modes of operation: below cutoff, above cutoff, and in the area of cutoff. Assuming that the amplifier has adequate frequency response beyond cutoff, the filter works as expected. At frequencies well above cutoff, the high-frequency model depicted in Figure 3 is used to show the expected circuit operation. The assumption made here is that $C1$ and $C2$ are effective shorts when compared to the impedance of $R1$ and $R2$, so the amplifier's input is at ac ground. In response, the amplifier generates an ac ground at its output limited only by its output impedance, Z_o . The formula shows the transfer function of this particular model.

Z_o is the closed-loop output impedance. It depends on the loop transmission and the open-loop output impedance, z_o :

$$Z_o = \frac{z_o}{1+a(f)b}$$

where $a(f)$ is the open-loop gain of the amplifier and b is the feedback factor. This feedback factor is constant—set by resistors $R3$ and $R4$. But the open-loop gain, $a(f)$, depends on frequency.



3. At frequencies well above cutoff, the high-frequency model shown here takes into account the non-ideal effect of the amplifier's output impedance. The ac ground at the amplifier's output is limited by its output impedance, Z_o .

$$\frac{V_o}{V_i} = \frac{1}{\frac{R1}{R2} + \frac{R1}{Z_o} + 1}$$

Assuming $Z_o \ll R1$

$$\frac{V_o}{V_i} = \frac{Z_o}{R1}$$

Equation 2

$$\frac{V_o}{V_i}(\text{LP}) = \frac{K}{s^2(R_1R_2C_1C_2) + s(R_1C_1 + R_2C_1 + R_1C_2(1-K)) + 1} \quad (2)$$

$$\text{where } K = 1 + \frac{R_4}{R_3}$$

With dominant-pole compensation, the amplifier's open-loop gain decreases by 20 dB/decade over the usable frequencies of operation. Assuming z_o is mainly resistive (usually a valid assumption up to a few hundred megahertz), Z_o increases at a rate of 20 dB/decade. The transfer function appears to be a first-order high pass.

At frequencies above 100 MHz (or so), the parasitic inductance in the output starts playing a role and the transfer function transitions to a second-order high pass. Plus, at higher frequency, the high-pass transfer function will roll off due to stray capacitance.

Simulation and lab data: To show the effects described above, a Sallen-Key low-pass filter was simulated in Spice and lab tested using a THS3001 operational amplifier from Texas Instru-

ments. The THS3001 is a high-speed, current-feedback amplifier with an advertised bandwidth of 420 MHz. Choosing $R_1 = R_2 = 1 \text{ k}\Omega$, $C_1 = C_2 = 1 \text{ nF}$, $R_3 = \text{open}$, and $R_4 = 1 \text{ k}\Omega$ results in a low-pass filter with $f_c = 159 \text{ kHz}$ and $Q = 1/2$.

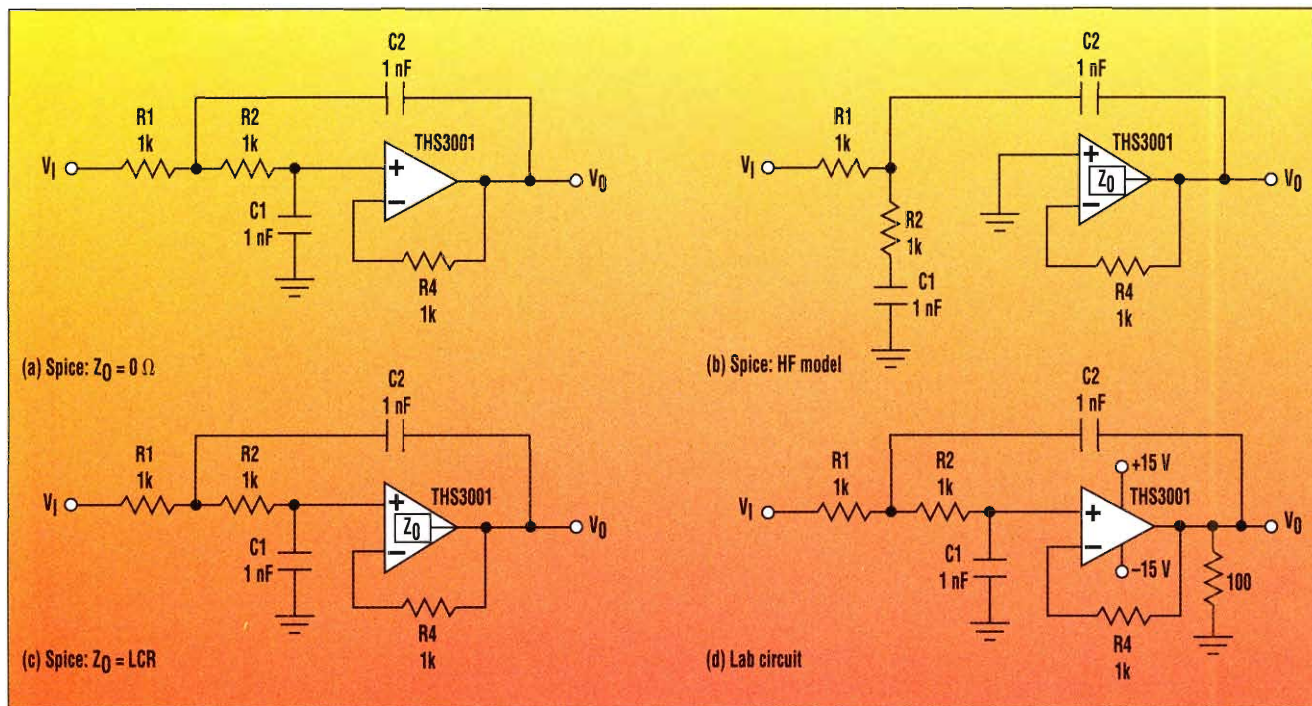
Figure 4a depicts the simulation circuit with the Spice model modified so that the output impedance of the amplifier is 0Ω . In Figure 5, curve (a) shows the frequency response as simulated in Spice. It also reveals that with zero output impedance, the attenuation of the signal continues to increase as frequency rises.

Figure 4b depicts the high-frequency model as exemplified in Figure 3, where the input is at ground and the output impedance controls the transfer function. The Spice model used for the THS3001 includes an LRC net-

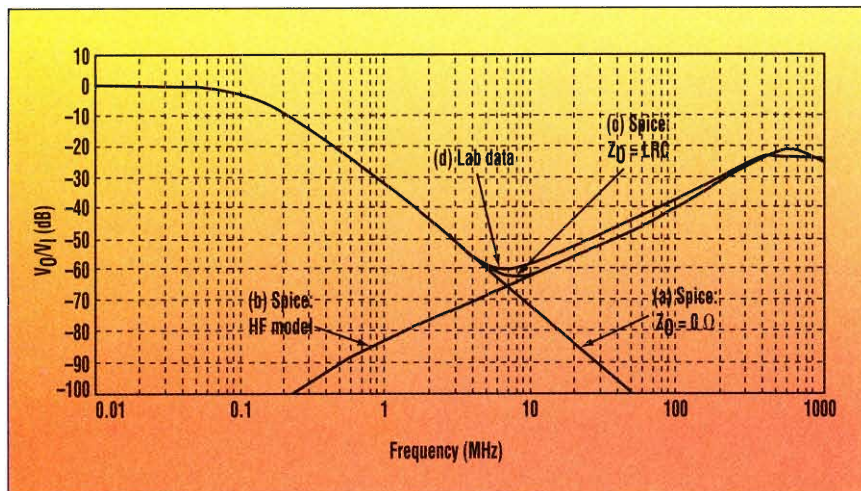
work for the output impedance. Again, Figure 5 shows the frequency response as simulated in Spice, but this time it's symbolized by curve (b). The magnitude of the signal at the output is seen to cross curve (a) at about 7 MHz. Above this frequency, the output impedance causes the switch in the transfer function, which is described above.

Look to Figure 4c for the simulation circuit using the Spice model with the LCR output impedance. Figure 5's curve (c) shows the frequency response for this model. With the output impedance, the attenuation caused by the circuit follows curve (a) until it crosses curve (b), at which point it follows curve (b). Figure 4d reveals the circuit as tested in the lab, with curve (d) in Figure 5 showing that the measured data agrees with the simulated data.

Comments about component selection: Until now, the choosing of resistor and capacitor values has been left without mention. Theoretically, any values of R and C that satisfy the equations may be used. But practical considerations call for certain guidelines to be followed. Given a specific corner frequency, the values of C and R are inversely proportional to one another.



4. For Spice simulation purposes, the filter was modeled with amplifier output impedance of 0Ω (a), a high-frequency model corresponding to Figure 3 (b), and a simulation circuit using the Spice model having an LCR output impedance (c). Actual test measurements were performed using a fourth circuit (d). Tests show that the measured data agrees with the simulated data, according to curve (d) in Figure 5.



5. The four curves show the frequency response of the circuits of Figure 4, as simulated in Spice. At frequencies above the intersection of curves (a) and (b) at 7 MHz, filter attenuation is degraded as the response, then it follows curve (b).

By making C larger, R becomes smaller and vice versa.

In the case of the low-pass Sallen-Key filter, the ratio between the output impedance of the amplifier and the value of filter component R sets the transfer functions seen at frequencies

well above cutoff. The larger the resistor's value, the lower the transmission of signals at high frequency. Making R too large may result in C becoming so small that the parasitic capacitors, including the input capacitance of the amplifier, cause errors. The best

choice of component values depends on the particulars of your circuit and the tradeoffs you're willing to make.

Here are some general recommendations for capacitors and resistors: Engineers should avoid capacitors with values less than 100 pF. If at all possible, use an NPO type. X7R is okay in a pinch, but avoid Z5U and other low-quality dielectrics. In critical applications, even higher-quality dielectrics, like polyester, polycarbonate, Mylar, etc., may be required. As for resistors, values in the range of a few hundred to a few thousand ohms are the best bet. You also should choose metal-film resistors that possess low temperature coefficients. Finally, use 1%-tolerance capacitors and resistors, preferably those of the surface-mount variety. □

Jim Karki is a systems specialist for Texas Instruments' precision analog products. He received his BSEE from the University of Washington, Seattle, and has been with TI for more than two years.

letters

READERS SPEAK OUT

Sallen-Key Filters Find More Limits

Another limitation not mentioned in the article [on Sallen-Key filters] is that the filter possesses a frequency response for amplifier-generated noise which is different from the filter characteristic modeled (*Dec. 17, 1999, p. 96*). In low-noise applications, the high "Q" of the filter magnifies the noise and can make the circuit unusable. Needless to say, this is not usually modeled in Spice.

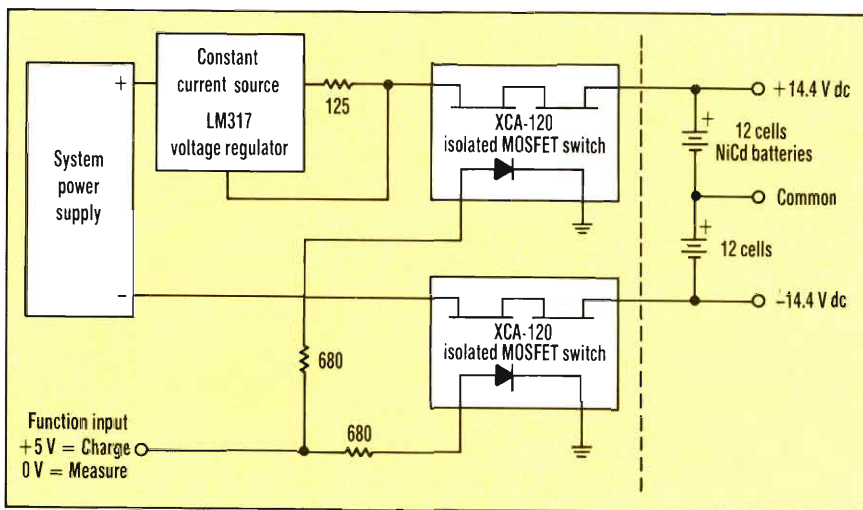
Replacing the op amp with a single low-noise emitter-follower transistor can improve both the noise performance and the cutoff behaviour described in the article, and is usually cheaper too! (An npn-pnp follower pair can reduce dc offsets when required.)

*Anthony New
Wireless Systems International
Bristol, U.K.*

CIRCLE
525 RID MEASUREMENTS
OF SUPPLY NOISE

STEVEN C. HAGEMAN

Calex Manufacturing Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523;
(415) 932-3911.



A CIRCUIT DESIGNED AROUND TWO XCA-120 isolated MOSFET switches charges a set of batteries, yet quickly isolates the instrument from the charging supply when making noise-sensitive measurements. When the Function Input is at 0 V, the MOSFET switches supply ± 200 -V peak isolation.

When very high gain-bandwidth amplifiers are required for seismic or vibration analysis, even the quietest linear power supply can create lots of noise. Improper isolation from the main power bus generates the noise, which in turn affects the measurements. This problem is further magnified if the instrumentation is mounted on a truck

or situated in a heavy-machinery testing laboratory.

Powering the instrumentation from batteries can eliminate the noise, but a connection to the main power bus is necessary for recharging. This design keeps the batteries charged from the main power bus, yet allows fast disconnection and high isolation from the bus when measurements are needed.

The heart of the charging system consists of two XCA-120 isolated MOSFET switches from the Theta-J Corp., Wakefield, Mass. The switches act as 15- Ω resistors when turned on; when turned off, they block 200 V peak ac or dc voltages.

A typical circuit could use 24 one-third AA nickel-cadmium batteries wired to supply a nominal voltage of ± 14.4 V dc to the measurement circuitry (see the figure). These particular batteries are rated at 100 mA-hours (100 mA for 1 hour or 10 mA for 10 hours).

When measurements aren't being made, the main power supply (greater than 40 V dc in this example) is connected to an LM317 voltage regulator set to a safe charge of 0.1 C or 10 mA. At this rate, the batteries will be fully charged in 10 to 11 hours and will stay at full charge for an indefinite period of time. During the charge cycle, the XCA-120s are turned on by a +5-V signal at the Function Input node line.

The input is set to 0 V when critical measurements are needed, which shuts off the XCA-120s in about 1 ms and supplies complete isolation to the measurement circuitry. The isolation is ± 200 V peak with 12 pF of total capacitance sent back to the system.

The 24 batteries take up less than 5 in.³ of space and can be packaged in a box that's 2.6 by 2.6 by 0.7 in. Additional linear regulation can be added after the batteries for better load and discharge regulation. \square

CIRCLE
526 TAKE THE JITTER
OUT OF PLLS

PATRICK CONWAY

28361 Plainfield Dr., Rancho Palos Verdes, CA 90274; (213) 541-6024.

Phase-locked loops (PLL) that use phase-frequency (P-F) detectors inherently have high jitter. The jitter is a result of the P-F detector's dead zone and the charge pump's inability to capture narrow pulses. Adding a D-type flip-flop phase detector can circumvent these problems.

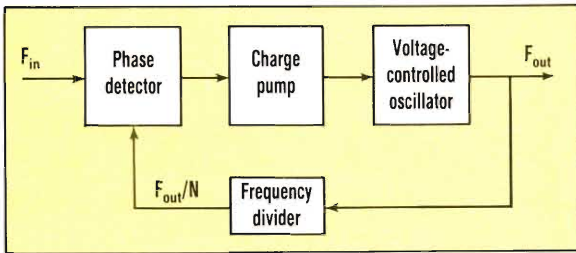
A PLL block diagram shows that the output frequency divided by N is compared to the input frequency in the detector (Fig. 1). The charge pump generates a voltage to control the voltage-controlled oscillator (VCO) so that $F_{out}/N = F_{in}$ at lock.

A typical phase detector is an MC4044 (TTL) or an MC12040 (ECL).

For ECL, the "Up" and "Down" outputs can be combined with two diodes to produce a three-level phase-error signal (Fig. 2). If the "Up" and "Down" outputs are inactive when using TTL, they're in a high-Z state and can be wired together. The reference voltage equals the average of the high and low levels. The value of load resistor R_1 is as low as the P-F detector can drive.

The P-F detector produces pulses whose width is proportional to the phase error. This causes charge to accumulate in the capacitor (hence the term charge pump). The capaci-

IDEAS FOR DESIGN



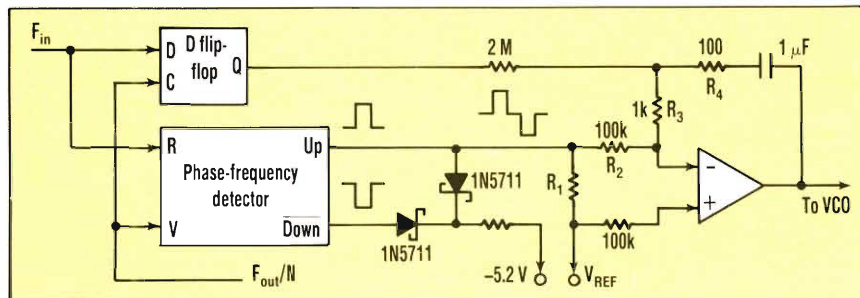
1. A PHASE-LOCKED loop block diagram shows that the output frequency is divided by N and compared to the input frequency in the phase detector.

tor and op amp combination make up an integrator, which produces the control voltage for the VCO. A film capacitor with low dielectric absorption (hysteresis) should be used.

A weak loop using a D flip-flop phase detector is added to sup-

ply a tight lock at the P-F detector's null. The loop acts as a bang-bang servo (the opposite of a proportionate servo), applying a small charging current to the capacitor in one of the two directions at all times. The jitter of this weak loop is considerably less than that of the P-F loop. Of course, the weak loop can't account for large initial errors. During acquisition, the loop has a negligible effect on the P-F loop. R_4 is the damping resistor for the D flip-flop loop, while $R_3 + R_4$ is the damping resistance of the P-F detector loop.

The component values shown in the circuit illustrate their orders of magnitude and they can be changed to satisfy performance requirements. The P-F detector loop can be analyzed using classical linear methods. The response of the D flip-flop loop using a step input can be simulated by calculating the loop error for each input-signal period. □

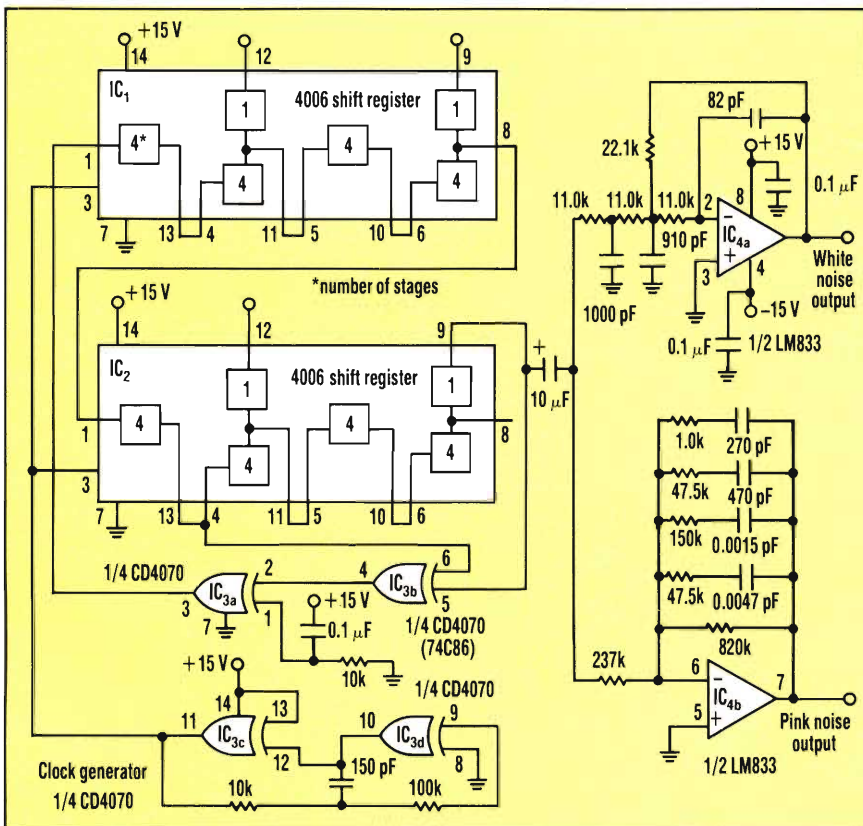


2. BY SUPPLEMENTING THE phase-frequency loop with a D flip-flop loop, the high jitter due to the dead zone of the P-F detector can be greatly reduced.

CIRCLE 522 CREATE AN ACCURATE NOISE GENERATOR

KERRY LACANETTE

National Semiconductor, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.



THIS WHITE and pink noise-generation circuit is based on a pseudorandom noise source consisting of two 4006 shift registers, NOR gates, a clock, and two active filters.

Make an accurate noise-generator circuit that produces white and pink noise from a digital pseudorandom noise source consisting of a pair of 4006 shift registers (IC_1 and IC_2) and four exclusive NOR gates (IC_3) (see the figure). White noise is characterized by constant spectral density per unit bandwidth, while pink noise has constant power in each octave or decade of frequency. Noise generators that yield such noise are useful in many applications. These include audio, acoustical, and audiological testing, loudspeaker burn-in, sound-effects generation, and dither for analog-to-digital converters.

There are 36 shift-register stages

available in the two shift registers. Using 33 stages generates the longest possible pseudorandom sequence from the two shift registers. The $0.1\text{-}\mu\text{F}$ capacitor and the $10\text{-k}\Omega$

resistor ensure that the circuit will always start with a few "1s" loaded into the register. If the circuit starts with all "0s," it will never produce an output. Built around half of IC_3 , the circuit's oscillator supplies a 330-kHz clock waveform. At this clock frequency, the repetition rate of the pseudorandom noise sequence is less than once every 25 hours.

The output of the pseudorandom sequence generator can be filtered to supply the type of signal desired. For example, a low-frequency band-pass filter can be applied to produce low-frequency noise for sound effects (earthquakes and other rumbling sounds), or subsonic frequencies can be useful as random-drive signals for shaker tables. The most commonly used noise signals, however, are those that contain white or pink spectral characteristics.

To convert the digital pulse train from the shift registers into an analog white-noise output, the pseudorandom sequence is filtered by a third-order active Butterworth low-pass filter with a 40-kHz cutoff frequency (IC_{4a}). The low-pass filter yields a flat noise spectrum that's down only 0.25 dB at 25 kHz.

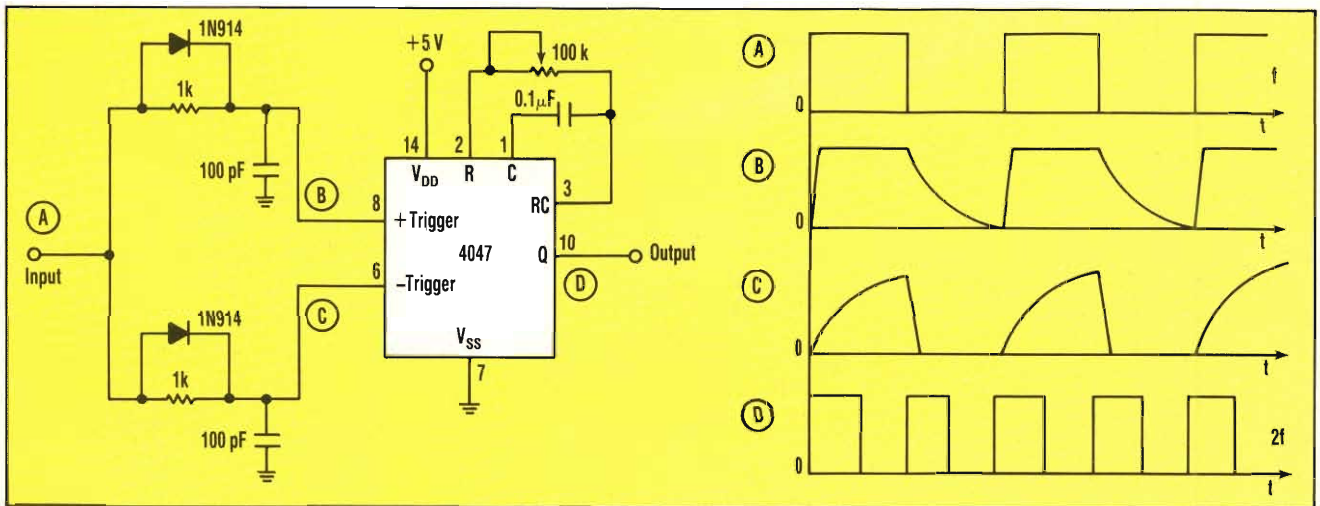
To produce pink noise, a random-noise signal must be filtered so that the noise power at each frequency increases with the inverse of frequency. Therefore, a 3-dB/octave roll-off rate is required. The pink-noise filter (IC_{4b}) uses alternating poles and zeros to approximate this slope. The accuracy of the pink-noise output spectrum using the values shown is better than ± 0.4 dB over the audio frequency range. □

CIRCLE 523 ONE IC DOUBLES FREQUENCY

V. LAKSHMINARAYANAN

Centre for Development of Telematics, Sneha Complex, 3rd Floor, 71/1 Miller Rd., Bangalore 560 052, India.

An inexpensive frequency doubler and duty-cycle-variation circuit can be designed around one IC—a monostable 4047 that's triggered directly by a low-to-high or high-to-low transition. The circuit uses two RC differentiators to detect the leading and trailing edges of a digital input signal (see the figure, left). The dif-



BY USING A MONOSTABLE 4047 and several external resistors, capacitors, and diodes, a simple frequency doubler can be constructed. Also the output duty-cycle can be varied up to 100% (left). The waveforms at points B and C indicate the charging and discharging of the two 100-pF capacitors. This shows at what points the 4047 is triggered (right).

ferentiators' transition spikes trigger the 4047 at both edges, effectively doubling the input-signal frequency (see the figure, right). The external potentiometer-capacitor combination at pins 1, 2, and 3 of the monostable IC can be varied to adjust the output pulse train's duty cycle up to 100%. □

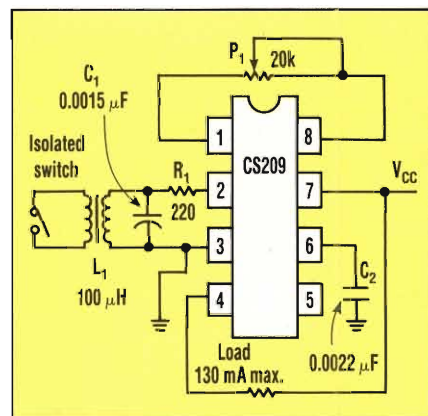
CIRCLE 521 CIRCUIT DETECTS SWITCH CLOSURE

NOOR SINGH KHALSA

EG&G Inc., EM Div., P.O. Box 809, MS E-1, Los Alamos, NM 87544.

A standard proximity detector circuit for the Cherry Semiconductor CS209 IC can detect an isolated switch closure by adding a few turns of wire around the circuit's inductor (Radio Shack 273-102). Moreover, the technique doesn't require any isolated power (see the figure, right). With

the switch open, the potentiometer P_1 is adjusted until the output switches off. When the switch is closed, the Q of the circuit changes and the output turns on. Capacitor C_1 should be silvered mica, and potentiometer P_1 should be a multiturn type such as the Bourns 3006P-1-203. A 9-V-supply can be used for V_{cc} . □



A STANDARD proximity detector can detect an isolated switch closure.

CIRCLE 522 BOOST MOSFET'S DRIVE CURRENT

KIM GAUEN

Motorola Inc., 5005 E. McDowell Rd., Phoenix, AZ 85008; (602) 244-6701.

Because MOSFETs are voltage controlled, they're usually very easy to drive. However, a problem arises when a power MOSFET is used as a high-side switch, such as when a load is connected to the MOSFET's source. Applications that require a high-side switch include solid-state ac or dc relays or H-bridge motor-control circuits. In these examples, it's difficult to reference the gate-drive circuit and gate-drive supply to the MOSFET's source.

Gate transformers, bootstrapped supplies, or optocouplers typically drive MOSFETs employed as high-side switches. For various reasons, these techniques create problems when the MOSFET must operate at high duty cycles or remain on continuously, as it might in a solid-state relay. An optocoupled gate drive performs well, but it requires an isolated supply referenced to the MOSFET's source. The isolated supply drives the MOSFET's gate.

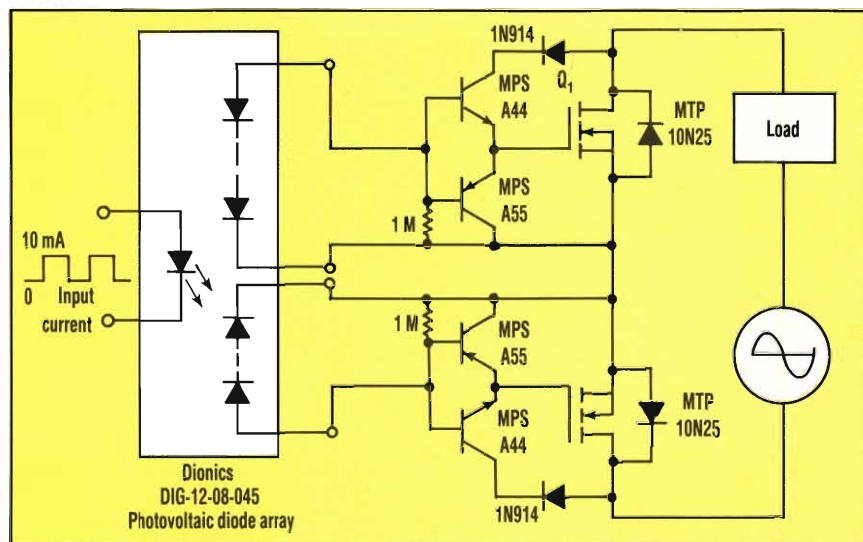
Photovoltaic diode arrays match up well when driving MOSFETs because they produce isolated output voltages of 5 to 10 V. But because their output current is so low ($\approx 5 \mu A$), the MOSFET's turn-on is sluggish and noise coupled to the gate

from the MOSFET's parasitic drain-to-gate capacitor can trigger undesirable switching. Buffering the array's output with a complementary emitter follower can improve system performance when using the photovoltaic diode array. The obvious drawback is that a floating-gate supply is still needed.

A clean and inexpensive way to eliminate the floating-gate supply is to use the voltage available at the MOSFET's drain to drive its gate

(see the figure, below). Tying the collector of Q_1 (a high-voltage, small-signal, 400-V npn) to the MOSFET's drain supplies sufficient gate-drive voltage when it's needed most—when the MOSFET's drain-to-source voltage is high. Two such circuits used back-to-back form an ac relay.

Using the emitter follower attached to the drain increases gate-drive current and decreases the MOSFET's turn-on time by a factor equal to the high-voltage npn's beta. The resulting drain-to-source voltage fall times depend on the MOSFET's size and its required gate charge. The circuit that's used gives a fall time of 200 μs for an MTP10N25 10-A, 250-V MOSFET. With such fall times cutting switching losses, pulse-width modulation at

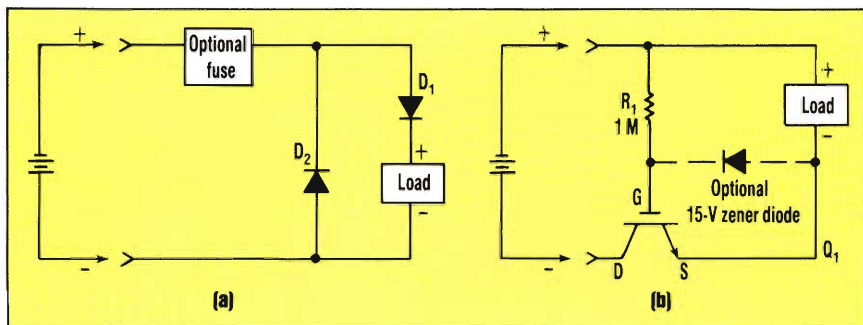


THE EMITTER-FOLLOWER buffer improves the MOSFET's switching speeds without an isolated gate-drive supply, an economical way to omit the floating-gate supply.

CIRCLE 521 PROTECTION CIRCUIT CUTS VOLTAGE LOSS

ROBERT A. PEASE

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051; (408) 721-5613.



ANTIREVERSAL PROTECTION is typically created by placing a rectifier at D_1 or D_2 (a). By using a MOSFET and a resistor instead, the voltage loss associated with the series diode is greatly reduced as are the unwelcome side effects associated with the shunt diode such as ruining the battery or blowing a fuse (b).

It's well known that connecting a battery (or power supply) with reversed polarity can damage or destroy almost any electronic unit. Consequently, many engineers add in a rectifier at diodes D_1 or D_2 (see the figure, a). D_1 prevents any damage in case of reversal, yet it also wastes more than half a volt of the supply voltage. D_2 doesn't waste any power during normal operation. But when it acts as a crowbar, it may ruin the battery or itself, or blow a fuse.

By replacing the diodes with one MOSFET and one resistor, these problems are avoided (see the figure, b). When the correct voltage is applied, the MOSFET turns on. If a large enough FET with low R_{on} is chosen, the voltage lost in the FET can be minimal. For example, with an inexpensive IRF 511 (under \$1 for a 5-A, 60-V, 0.6- Ω N-channel FET), the lost voltage drop can be as small as

60 mV, even with a 100-mA load.

If the battery is reversed, the FET is inherently turned off and no current flows. The value for R_1 isn't crit-

ical, but 100 k Ω or larger would be a good choice because it will prevent large transients from arriving at the V_{GS} . If the battery voltage is much larger than 15 V, a zener diode from the gate to the source is advisable to prevent overvoltage abuse of the gate. The circuit will then tolerate any voltage up to the breakdown V_{DSS} rating of the FET.

The circuit can use P-channel FETs if the polarity is inverted, making it possible to keep a common ground bus for two or more protected supply voltages. There are many variations on what can be done, starting with this basic circuit. Note that the current will flow through the MOSFET in reverse of the normal direction. If the drain and the source weren't reversed from the ordinary connection, the FET wouldn't turn off. □

ELECTRONIC DESIGN wishes to advise its readers that National Semiconductor has applied for a patent. National Semiconductor has a patent pending on this circuit.

CIRCLE 522 ENCODER AIDS DATA TRANSMISSION

MAREK A. KONARSKI

Northern Telecom Canada Ltd., P.O. Box 6135, Montreal, Quebec, Canada H3C 3S1; (514) 331-9611.

In a digital-transmission hierarchy, DS-1, DS-2, and DS-3 are return-to-zero (RZ), 50% duty-cycle bipolar signals. Bipolar binary data is represented by three amplitude levels: "0," "+," and "-." When coding, a binary zero is coded as 0, but a binary one can be represented by either a + or a -. The + represents a rise from 0, while the - represents a fall. Consecutive positive or negative amplitudes are called bipolar violations because they violate the bipolar rule.

Long strings of zeros are associated with the absence of transitions, making clock recovery difficult. To eliminate these long strings, a bipolar signal can be coded. One common coding scheme is called bipolar-with-

N-zero-substitution (BNZS). BNZS means that N consecutive zeros are replaced with an N-bit pattern that consists of binary 0 bits, binary B bits (data 1), and binary V bits (data 1) violating the bipolar rule. The encoding is applied on the transmit side of the digital multiplexer.

A B3ZS (bipolar-with-3-zero-substitution) encoder replaces each group of three consecutive zero bits with a sequence of B0V or 00V. The choice between B0V and 00V is made so that an odd number of B pulses

IFD WINNERS

IFD Winner for February 22, 1990

James A. Kuzdrall, Intrel Service Co., Box 1247, Nashua, NH 03061; (603) 883-4815. His idea: "Voltage Divider is Ultra-Stable."

SUBSTITUTE ENCODED DATA

Digital Data	1 0 0 0 1 0 1 0 0 0 1 0 0 0
Bipolar Code	+ 0 0 + - 0 + - 0 - + 0 0 +
Violation Code	V B V V

Accordingly, 32° can be added to the display (reading in °F) when R₃ is adjusted until V_{in-} is 0.17776 V more negative than the converter's ana-

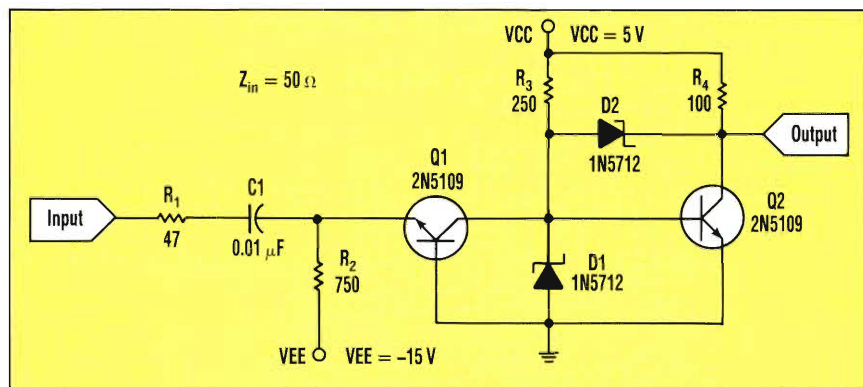
log-common input. In the °C measurement mode, resistors R₁, R_{2a}, and R_{2b} divide the LM35 output by 5/9. Therefore, the converter doesn't

need to change its V_{REF} to switch the display reading from °F to °C. The LCD automatically reads correctly in °C. □

CIRCLE 525 INTERFACE 50-Ω RF To HC/HCT LOGIC

MICHAEL A. WYATT

SSAvD Honeywell Inc., 13350 HW 19 South, Clearwater, FL 34624-7290; (813) 539-5653.



THIS AMPLIFIER OPERATES beyond 30 MHz with a 10-dBm (1 Vpk) low-impedance rf input signal and easily drives HC and HCT types of logic families.

To interface 50-Ω rf and CMOS circuits, an amplifier must maintain a constant input impedance as the frequency changes and it must supply a

full 0-to-5-V output swing. An amplifier consisting of two transistors and a pair of diodes can do the job (see the figure). The amplifier operates beyond 30 MHz with a 10-dBm (1 Vpk)

rf input signal and easily drives HC and HCT types of logic families.

In the circuit, Q1 operates in a common-base configuration, enabling a low-input impedance and high-frequency response. Resistor R₂ sets Q1's emitter current to 19 mA, producing an effective emitter impedance of less than 2 Ω. Q1's emitter impedance can be calculated by the kT/qI_e relationship, where k is Boltzmann's constant (1.38E-23 J/K), T is temperature in degrees Kelvin, q is electron charge (1.602E-19 C), and I_e is the emitter current.

Resistor R₁ becomes the effective amplifier input impedance because of the low Q1 emitter impedance. Schottky diode D1 limits the negative voltage swing at Q1's collector to -0.6 V, which keeps the collector-to-base junction from becoming forward-biased. Schottky diode D2 serves the same function for Q2, which has a common-emitter-amplifier configuration. Neither transistor saturates (forward collector to base junction) on positive or negative signal swings. This feature keeps transistor storage-time effects to a minimum. □

CIRCLE 526 DIVIDE-BY-3 CIRCUIT HAS 50% DUTY CYCLE

WALTER P. SJURSEN

Base Ten Systems Inc., One Electronics Dr., Trenton, NJ 08619; (609) 586-7010.

Only one 74HC7074 IC is needed to divide an input clock frequency by three and supply an output duty cycle of 50%. The IC contains two D-type flip-flops, one NAND gate, one NOR gate, and two inverters (see the figure). The inverters can implement an oscillator to supply the input signal.

The input signal (CLK_{IN}) is a square wave with a 50% duty cycle. Initially, the signals CLK_{IN} and CLK_{OUT} and node A are all in a

logic-low state, while node B is high. At the first low-to-high transition of CLK_{IN}, node A toggles high, which clocks the second flip-flop and causes CLK_{OUT} to toggle high. At the second low-to-high transition of CLK_{IN}, node A toggles low. When CLK_{IN} returns low, node B is forced low as well.

The low at node B sets the output of the first flip-flop high (node A toggles high) which clocks the second flip-flop and sends CLK_{OUT} low.

The high logic level at A forces B to a high level. The next low-to-high transition of CLK_{IN} toggles A low, and the sequence repeats.

The duty cycle of CLK_{OUT} is given by the equation:

$$D_{out} = (T_{in} + T_{in} - D_{in} + \Delta t_{PD}) / 3T_{in}$$

where T_{in} is the period of CLK_{IN}, D_{in} is the duty cycle of CLK_{IN}, and Δt_{PD} is the difference in rising- and falling-edge propagation delays.

The rising-edge delay is the time from the rising edge of CLK_{IN} to that of CLK_{OUT}. It is made up of the delays through the two flip-flops. The falling-edge delay is the time from the falling edge of CLK_{IN} to the falling edge of CLK_{OUT}. The falling-edge delay consists of the de-

quencies from 1 kHz (determined by the 0.1- μ F input capacitor) to greater than 100 kHz (limited almost exclusively by the analog switch's fre-

quency response capability). The comparator threshold voltage V_{REF} and the cutoff frequency f_C determine the frequency resolution. \square

eliminate these aliasing frequencies (see the figure). The circuit attenuates the aliasing products by more than 60 dB, thus preventing substantial distortion at the output. The balanced amplifier eliminates the need for a symmetrical carrier and highly symmetrical switching in the LM1496 to suppress the aliasing frequencies. While the circuit could also use a balanced transformer instead, the balanced CA3139 op amp is the more cost-effective solution. \square

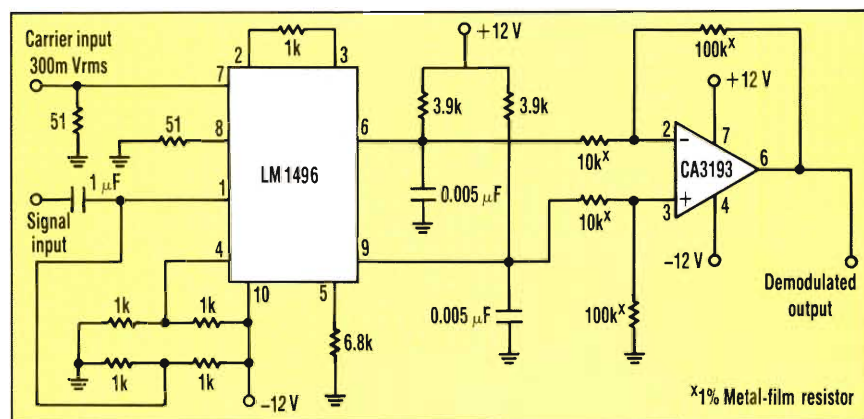
CIRCLE 522 REDUCE DISTORTION IN MOD-DEMOD CIRCUIT

V. LAKSHMINARAYANAN

Centre for Development of Telematics, Sneha Corp., 71/1 Millers Rd., Bangalore 560 052, India.

The LM1496, a balanced modulator-demodulator, produces an output voltage proportional to the product of a signal, f_s , and a carrier, f_c , input. Unfortunately, the suppression of the carrier signal by the LM1496 at its output is poor even within its specified band of operation, especially at high frequencies. Also, aliasing frequencies of even multiples of f_C plus or minus even multiples of f_s ($2f_C \pm 2f_s$) cause serious in-band spurious interference.

A CA3193 BiMOS op amp, configured as a balanced differential amplifier at the output of the LM1496, can



THE BALANCED OP-AMP CIRCUIT at the output of the LM1496 attenuates aliasing output products by more than 60 dB.

CIRCLE 523 OP-AMP MONITORS LIQUID LEVELS

DONALD WILCHER

General Motors Corp., 2625 Tyler Rd., Ypsilanti, MI 48197; (313) 481-4858.

Industrial processes use many types of liquids that often require a way to detect their levels in a confined space or container. A simple method uses a common 741 operational amplifier configured as a comparator and a low-cost npn transistor as an output driver (see the figure).

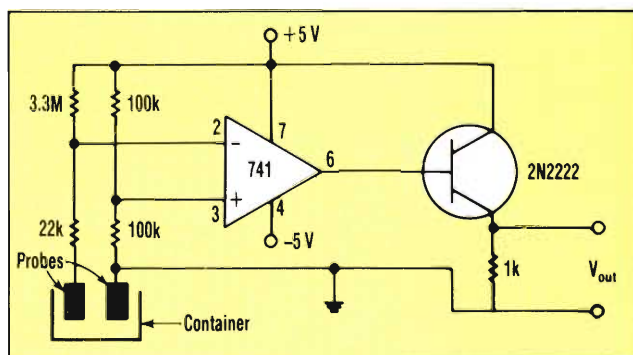
In the circuit, with no liquid detected, a voltage of about 2.92 V is present at the op amp's inverting input (pin 2), which is established by the 3.3-M Ω and a 22-k Ω resistor combination. Two 100-k Ω resistors establish a reference voltage of +2.5 V at the noninverting input (pin 3) of the op amp. Under those conditions, the op amp's output is -3.56 V, which

keeps the 2N2222 transistor turned off and the voltage across its 1-k Ω output load resistor at 0 V.

When liquid reaches the probes, the 3.3-M Ω and 22-k Ω resistor circuit conductively connects to ground. When enough current (about 1.4 μ A) flows through the liquid, the small 30-mV drop developed across the 22-k Ω resistor drives the op amp to deliver an output

voltage of about 4.42 V. This voltage then drives a 2N2222 transistor into saturation, which generates a voltage drop of about 3.86 V across its 1-k Ω output load resistor.

This output voltage can drive an alarm status indicator—either a light or a tone generator. With the proper circuit interface and software, this circuit can act as an input to a sophisticated computer liquid-level monitoring system. \square



A COMMON 741 OP AMP and a low-cost npn transistor act as an input to a computer liquid-level monitoring system.

CIRCLE 521 SYNC DETECTOR'S FAILURES CUT

ISRAEL YUVAL

ADA (Israel), P.O. Box 2250, Haifa, Israel.

A synchronous detector circuit passes signals of only a specific frequency. When the input frequency f_1 is equal to the switching frequency f_s of the detector, the output equals $K\cos\phi$ —a constant representing a

dc level—where ϕ is the relative phase of the two frequencies. For f_1 close to f_s , the difference between them, $f_1 - f_s$, is a low-frequency beat. A low-pass filter in the circuit then determines the passband.

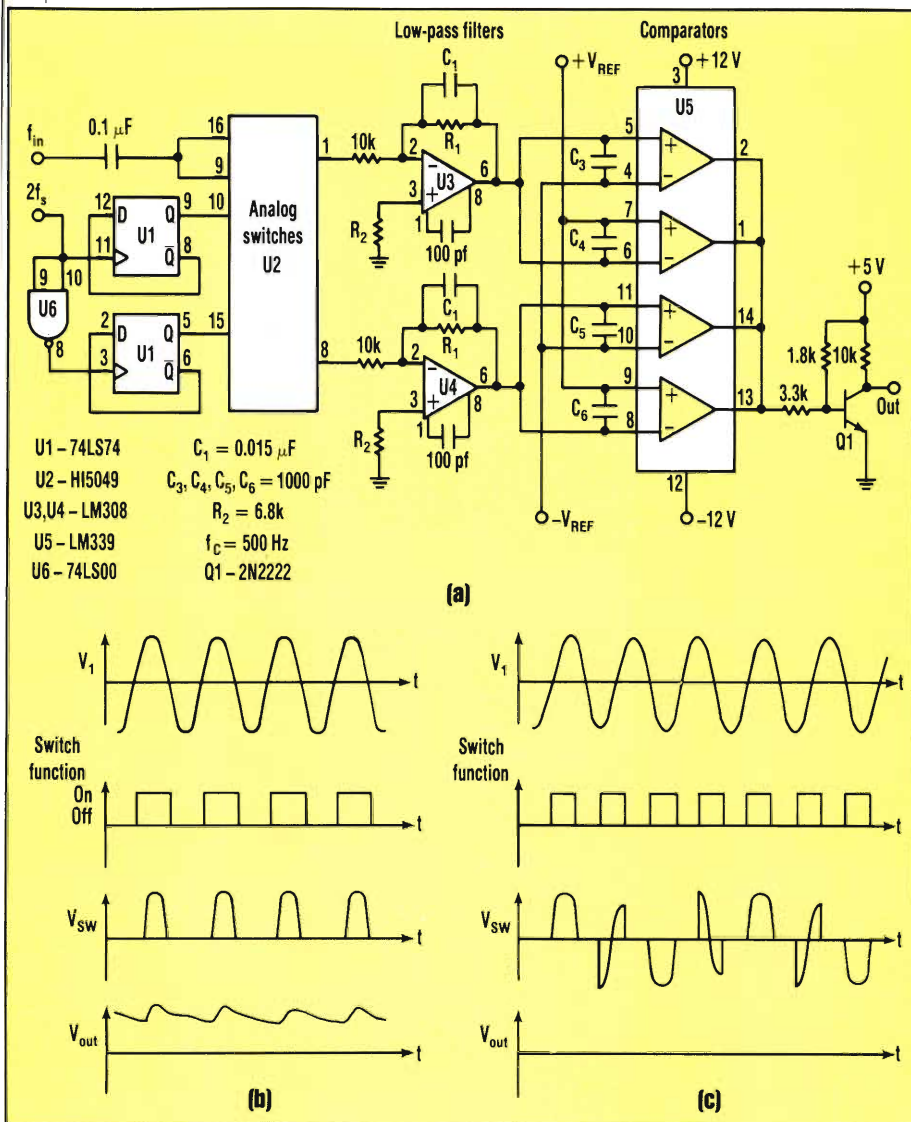
A problem arises, however, when

the phase difference (ϕ) between the two frequencies is 90° and the two frequencies are equal—the circuit output is zero, resulting in detection failure. Adding a quadrature channel in parallel with the main channel and ORing the outputs of the two quadrature circuits, however, eliminates the possibility of detection failure. When the output of one channel is zero, the output of the other channel is maximum.

In a practical circuit, two U1 flip-flops and inverter U6 generate the quadrature shift between the switching signals of the two parallel channels (see the figure). U6 inverts a square wave of frequency $2f_s$. Both U1 flip-flops divide the original and inverted waveforms by two, which then feeds into an HI5049 dual-analog switch U2. The parallel outputs from U2, which represent the difference between the input and switching frequencies, then feed into identical low-pass filters U3 and U4. Their 3-dB-down points, or cutoff frequencies f_c , equal $1/2\pi R_1 C_1$.

Finally, the signals pass into parallel, dual-bipolar comparators—U5. Bipolarity is essential because the resulting comparator inputs can either be positive or negative voltages when f_1 equals f_s . The U5 outputs are all wire-ORed and connected to the output transistor Q1, which serves as a level shifter and inverter. A high output from Q1 means that $f_1 - f_s$ is less than the cutoff frequency.

This circuit responds to input fre-



THIS FREQUENCY-DETECTOR CIRCUIT responds to input frequencies from 1 kHz to greater than 100 kHz (a). A high output from Q1 means that $f_1 - f_s$ is less than the cutoff frequency f_c of the low-pass filters (b). The comparator threshold voltage V_{REF} and the low-pass filter's cutoff frequency f_c determine the circuit's frequency resolution. Above f_c , the output approaches zero (c).

IFD WINNERS

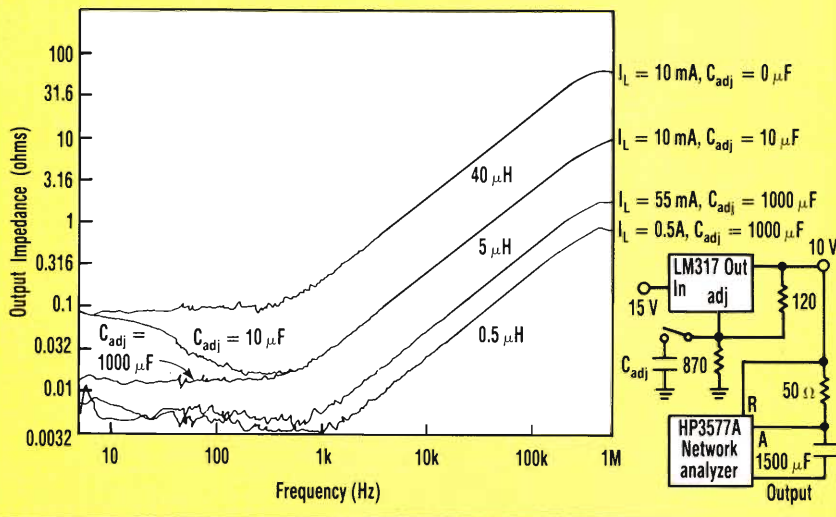
IFD Winner for
 March 13, 1989

Gene Davis, 7308 Rochelle Way,
 Fair Oaks, CA 95628. His idea:
 "Spreadsheet Simulates Logic."

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OUTPUT IMPEDANCE



2. THE OUTPUT IMPEDANCE of three-terminal regulators versus frequency forms a family of curves, one for each current level, which changes the output inductance.

cuit is extremely sensitive to excess noise from the supply at a particular frequency, then users can easily engineer the regulator's circuit so that the noise peak falls outside the critical range. Capacitors between 0.1 to 20 μF , especially those with low

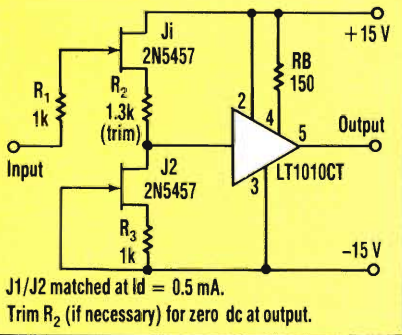
ESR, should be avoided in low-noise applications. The most effective noise reduction occurs with electrolytic capacitor sizes of 50 μF or greater connected across the output and at least 1 μF connected from the adjust pin to ground. \square

523 LOW DISTORTION VIDEO BUFFER

WALT JUNG and RICH MARKELL

Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035-7487; (408) 432-1900.

MATCHED JFETS



THIS LINEAR buffer amplifier's overall harmonic distortion is a low 0.01% or less at 3-Vrms output into a 500- Ω load with no overall feedback.

Wideband, unity-gain buffers are utilitarian elements for a broad spectrum of circuits, from dc to video frequencies. To execute a buffer, designers can use various approaches, employing one IC or a complex multitransistor discrete circuit. Of course, designers must typically trade-off in one or more areas, such as in dc offset, speed, linearity, and many other circuit parameters. Nevertheless, a buffer circuit using an LT1010CT video amplifier offers an interesting combination of high performance and relative simplicity.

The amplifier offers a 100-V/ μs

slew rate, a 20-MHz video bandwidth, and 100 mA of output. It has internal short-circuit protection and is relatively easy to use. For especially high-linearity applications, the amplifier can extend class-A operation by using a fifth biasing terminal. In Sallen-Key unity-gain types of active-filter, or even just for general audio use, this extended linearity can be very important.

One accommodation that designers must make, though, is to cancel the LT1010's nominal dc offset of approximately 60 mV. Also, its input impedance needs boosting. Accordingly, the LT1010 is primarily an inside-the-loop op-amp—not a pure standalone unity-gain buffer. Such accommodations make it possible to exploit the device's high output-drive and linearity virtues, and have a circuit with very high input impedance, low bias current, and low dc offset voltage.

In the circuit, a pair of JFETs, J1 and J2, are preselected for a nominal match at the bias level of the linearized source-follower input stage, at about 0.5 mA (see the figure). The source-bias resistor, R_2 , of J1 is somewhat larger than R_3 so that it can drop a larger voltage and cancel the LT1010CT's offset. In use, J1 and J2 provide an untrimmed dc offset of ± 50 mV or less. Then swapping J1 and J2 or trimming the R_2 value can give a finer match. If resistors R_2 and R_3 were equal, as in the case of classic form of a zero-offset FET buffer, the LT1010CT's offset in the second-stage would still appear at the circuit's output.

The circuit's overall harmonic distortion is low—0.01% or less at 3-Vrms output into a 500- Ω load with no overall feedback. Even with no overall feedback, the circuit's response to a ± 5 -V, 10-kHz square wave input, band limited to 1 μs , has no overshoot. If needed, setting bias resistor R_B lower can accommodate even steeper input-signal slopes and drive lower impedance loads with high linearity. The main trade-off for both objectives is more power dissipation. A secondary trade-off is the need for retrimming the source-bias resistor R_2 . \square

tiometer inserted between the two R resistors and connecting the wiper to the -A1 input can reduce the gain error. This adjustment can achieve an error of less than 0.1% before temperature coefficients introduce diminishing returns.

Voltage compliance for a current source defines the range of voltage over which its load can vary without disturbing linear operation. With common-mode and supply-rejection

ratios around 100,000 for the OPA2111 dual op amp, and a line regulation of $50 \mu\text{V}/\text{V}$ for the reference, the circuit develops an output resistance of $12,500 \times R_s$, or 31 M Ω . The result is a negligible 0.032-ppm output error for a full-scale output-current transition. Also, with the 2.5-V reference and the two OPA2111 amplifiers, normal operation is retained to within 6.5 V of the power-supply rail levels. □

three times greater than that of the same value of tantalum capacitor with an ESR of 1 to 2 Ω . The noise peak also reflects back to the input of the regulator at about 20-dB down from the output.

A little known fact is that the output impedance of three-terminal regulators varies substantially with load current and the programmed output voltage. As load current increases, the transconductance of the regulator's output transistor also increases. This behavior, in turn, causes the output inductance to decrease until the current-limit, bond wire, and lead resistances dominate the output impedance (Fig. 2). Consequently, although many designers have assumed that output impedance versus frequency was one curve, it's actually a family of curves—one for each current level. This phenomenon occurs in both positive and negative regulator types (LM117 and LM137), in adjustable and fixed types (LM140 and LM120), and in high- and low-current regulators (LM138 and LM317LZ).

Fortunately, in most cases, several microvolts of power-supply noise peaking at 5 or 10 kHz won't cause problems. But if the application cir-

CIRCLE 522 REDUCE NOISE IN VOLTAGE REGULATORS

ERROLL DIETZ

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5619.

Simply placing capacitors across the output and the adjust pins of three-terminal regulators is the usual approach to reducing regulator noise. On most regulators, though, the noise voltage over some narrow frequency ranges can peak—even though for typical values of output bypass capacitances, the overall noise voltage over a broad frequency range may drop. Also, the regulator's transient response can experience unexpected effects.

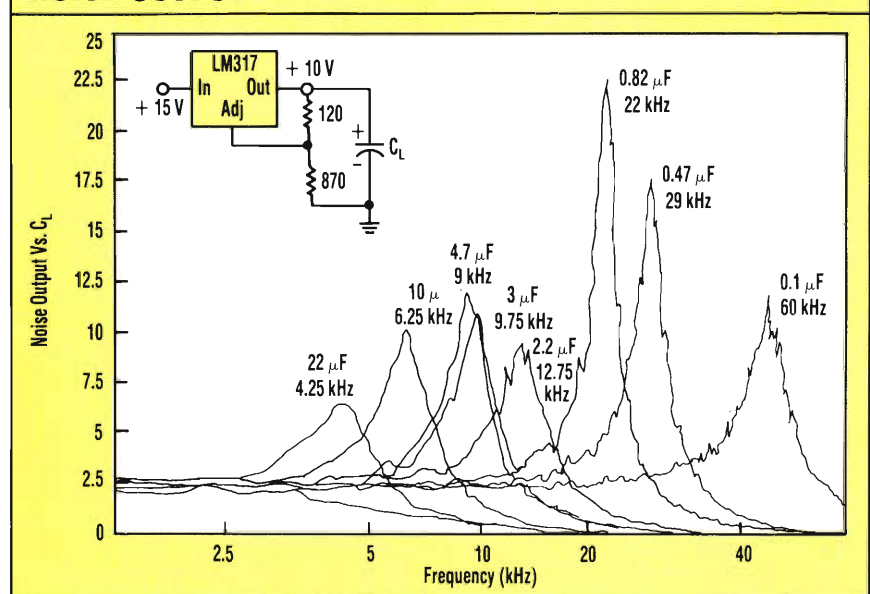
The output impedance of the LM317 voltage regulator, for example, over a 1-kHz to 1-MHz range, is inductive. This is not because of lead inductance, but rather because its internal gain roll-off is 6 dB/octave—just as for an op amp. This characteristic is typically unimportant to average users of IC regulator circuits. But when users shunt this inductive output impedance to ground with a capacitor, the combination can produce a noise peak at the resonant frequency of this inductance and added capacitance (Fig. 1).

For an LM317 with various capacitive loads, the frequency range of the noise spike doesn't extend much above 100 kHz nor below 10 kHz. This is because of ohmic losses in the inductance of the regulator and in the added output capacitance. The frequency is predictable from

$1/2\pi\sqrt{LC}$. This information can be scaled and also applied to all other three-terminal voltage regulators.

A noise spike's magnitude depends on the Q of the resonant circuit, which the series resistance of the output capacitor mainly dominates. For instance, a good 1- μF polypropylene capacitor with an equivalent series resistance (ESR) of 20 m Ω at 30 kHz produces a noise peak

NOISE OUTPUT



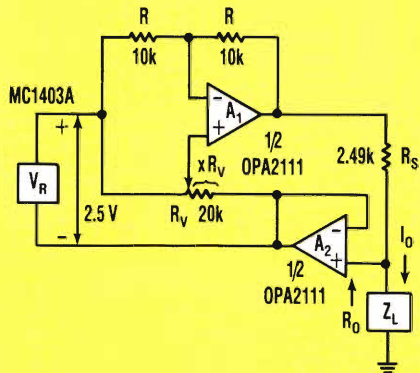
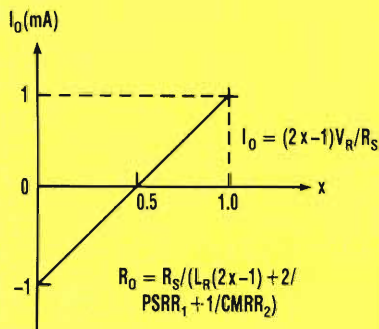
1. SHUNTING THE INDUCTIVE OUTPUT IMPEDANCE of a three-terminal regulator to ground with a capacitor can produce a noise peak at the resonant frequency of this inductance and added capacitance.

CIRCLE 521 BIPOLAR SOURCE USES UNIPOLAR REFERENCE

JERALD GRAEME

Burr-Brown Corp., International Airport Industrial Pk.,
P. O. Box 11400, Tucson, AZ 85734; (602) 746-7412.

BIPOLAR REFERENCE SOURCE



A CURRENT SOURCE that has continuous control of the magnitude and polarity of its amplifier gain needs only one voltage reference.

Conventional bipolar current-source circuits have one or more of three general limitations: the need for a variable-polarity voltage reference, the presence of large errors around zero current, and the requirement of a floating load. However, switching the polarity control of the circuit from its reference to its output amplifier's gain directly removes the first limitation and avoids the other two as well.

Changing the polarity of the dc reference source is the more direct means for obtaining a bipolar capability in a current source. But such a conventional approach requires two voltage references. Unfortunately, the two references would supply counteracting effects that are difficult to balance around the zero-current output level. Instead, a current-source circuit that has continuous control of the magnitude and polarity of its output-amplifier gain would need only one voltage reference.

Such an improved current-source circuit includes a reference V_R , a voltage-amplifier circuit A1 with a gain-setting resistor R_S , and a bootstrap follower amplifier A2 (see the

figure). The bootstrapping converts the circuit to a current source and allows the load to be grounded. Any voltage developed across the load Z_L feeds back to the reference and voltage amplifier, making their functions immune to that voltage. Then the current-source circuitry floats instead of the load.

To understand how the circuit works, consider both the input and output of voltage follower A2 grounded—zero voltage is convenient for the basic analysis. The grounded input and output points thus share a common potential throughout the voltage-follower action. Now the reference V_R and the gain of the A1 circuit control both the voltage across R_S and the magnitude and polarity of the current in R_S . The result is precise R_S current.

Connecting the voltage reference to both the inverting and noninverting inputs of A1 provides a balanced combination of positive and negative gain. The inverting connection has equal feedback resistors R for a gain of -1 , and the noninverting connection varies according to the fractional setting X of potentiometer R_V . Adjusting X controls the noninverting

gain and counters the effect of some of the inverting gain. The value of X is the portion of R_V 's resistance from the noninverting input of A1 to the temporarily grounded output of A2.

With the output of A2 grounded and $X=0$, the noninverting connection of A1 has no gain. The net gain V_R receives is the -1 of the inverting connection, and a voltage equal to $-V_R$ develops across sense resistor R_S , which develops an output current of -1 mA when V_R is 2.5 V.

At the other potentiometer extreme, when $X=1$, V_R connects to the noninverting input part of the A1 circuit to produce a gain of $+2$. Combined with the -1 gain of the inverting connection, the result is a net $+1$ gain. The voltage developed across resistor R_S is equal to $+V_R$ for a $+1$ -mA output to the load.

Between these potentiometer extremes, the current varies with X from -1 mA to $+1$ mA. The linearity and resolution are determined mostly by potentiometer errors. Simple multiturn potentiometers have errors around 1%; precision versions reduce the errors to about 0.1%. The tolerances and temperature coefficients of the fixed resistors and the voltage reference primarily determine gain errors. With an MC1403A reference and 1% metal-film resistors, the worst-case tolerance error is 4%. Trimming the inverting-gain part of the circuit with a 500- Ω poten-

CIRCLE 524 FEEDBACK CIRCUIT CLAMPS PRECISELY

JERALD GRAEME

Burr-Brown Corp., International Airport Industrial Park, P.O. Box 11400, Tucson, AZ 85732; (602) 746-7412.

A limiter circuit consisting of an input buffer (A1), an output-scaling amplifier (A2), two zener diodes (Z1 and Z2), and several other components can supply sharp, precise, bipolar clamp levels with continuous variable control, from 0 to ± 11 V (see the figure). A feedback loop enclosing the amplifiers and zeners generates the high clamping accuracy.

Within the limit range of the clamp ($\pm V_L$), the zener diodes are off, and A2 feeds back its output to the inverting input of A1 through R4. At the same time A1 drives A2 through the voltage divider Rv. The feedback forces the inverting input of op amp A1 to equal E1 at the noninverting input terminal.

The circuit forces the inverting input of A2 also to follow E1. There's no signal voltage drop across R4, because no current can flow from it into A1's inverting input. Consequently, the noninverting input of

A2, which defines the potentiometer output at feedback equilibrium, must also track E1. A resistor voltage divider can replace the control potentiometer Rv in fixed-level limiting applications.

Amplifier A2 then delivers an output:

$$E_O = (1 + R_3/R_2)E_1$$

when

$$-V_L < E_O < V_L,$$

and

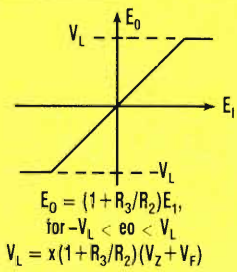
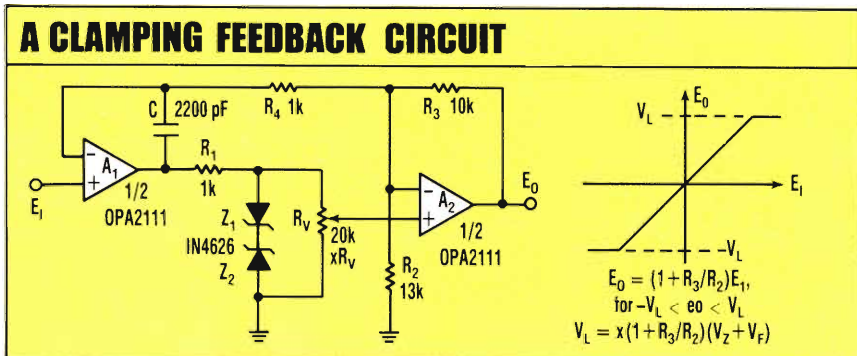
$$V_L = x[(1 + (R_3/R_2))(V_Z + V_F)]$$

where x is the setting fraction of Rv, and VZ and VF are the zener and forward voltages, respectively. The overall circuit response, then, is simply that of a voltage amplifier when the output signal is within the limit boundaries.

Amplifier A1 generates small deviations from an ideal response, because A2's circuit gain (1+R3/R2) amplifies any offset voltage and noise from A1. But the circuit's common feedback reduces any errors from A2's own offset or noise by the loop gain of A1. Similarly, this loop gain mitigates the clamping error by sharpening its clamping response. The zener drive increases during the transition to the clamping state.

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Morris Grossman, Ideas-for-Design Editor, Electronic Design, 10 Holland Drive, Hasbrouck Heights, NJ 07604.



AMPLIFIER A1 BUFFERS and amplifier A2 scales input signals under feedback control. Zener diodes and a potentiometer or voltage divider in the feedback loop supply a continuously variable bipolar-clamping limit.

VOTE!

Read all the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a \$150 Best-of-Issue award and becomes eligible for a \$1,500 Idea-of-the-Year award.

In the clamping mode, when the voltage across the two zeners reaches $\pm(V_Z + V_F)$, the circuit goes from acting as a voltage amplifier to acting as a voltage reference; the voltage across Rv is fixed and the potentiometer output is $\pm x(V_Z + V_F)$. Further increase in the magnitude of the signal at E1 can't change this potentiometer value, until it drops below the limit point, VL.

Thus, clamping is no longer limited to the fixed levels of available zener voltages. Even clamping levels as low as 5 mV become practical when offset-trimmable OPA111 op amps replace the OPA2111. However, available zener voltages and the closed-loop gain of A2 set the maximum clamping level.

Use of 10-V zeners and a gain of one for A2 can cover the voltage range of most analog-signal processing. Unfortunately, the voltage temperature coefficients of 10-V zeners would produce thermal drift in the clamping level. With 5.6-V zeners, however, the temperature coefficients of the zener and forward voltages tend to cancel. For such zener diodes $V_F + V_Z = 6.2$ V, and the net drift is near zero. Then, with A2 set to a gain of 1.77, the maximum limit voltage VL is 11 V.

The 5% tolerances of the zener voltages determine the basic accuracy of the clamp levels. The gain-setting resistors R2 and R3 impose additional tolerance error. However, adjusting the gain with these resistors can compensate for any zener-voltage error and resistor tolerances. With matched zeners, the adjustment can readily reduce the clamp-level errors to less than 1%. Without matching, the 5% error of simple zener clamping prevails, but the circuit

IDEAS FOR DESIGN

still clamps sharply.

For frequency stability, resistor R_4 and capacitor C supply a frequency roll-off in A1. At high frequencies, the capacitor shorts the output of A1

to its inverting input. Then A1 and A2 operate with independent feedback loops, and the overall circuit requires stability in the individual amplifiers. □

off-hook tone, the 440- and 480- Hz ringing tone, and the 480- and 620-Hz busy tone.

Such a circuit has wide applications for precise detection of the supervisory tones in exchanges. The

parator's inverting input controls the trigger point at which that comparator flips, and thereby can adjust its output timing relative to the other comparators. As a result, programming a correction code into the eight latches included in an AD7228 for each of its d-a converters can deskew the signals to the pin drivers (Fig. 2).

The best way to ramp the codes to the d-a converters up or down until the signals attain the correct timing relationships is with a counter circuit. Though a host microprocessor could load the codes, that would tie up the host too long—it could more profitably perform other tasks in that time. Once set, the d-a converter codes need no adjustment until the next calibration cycle.

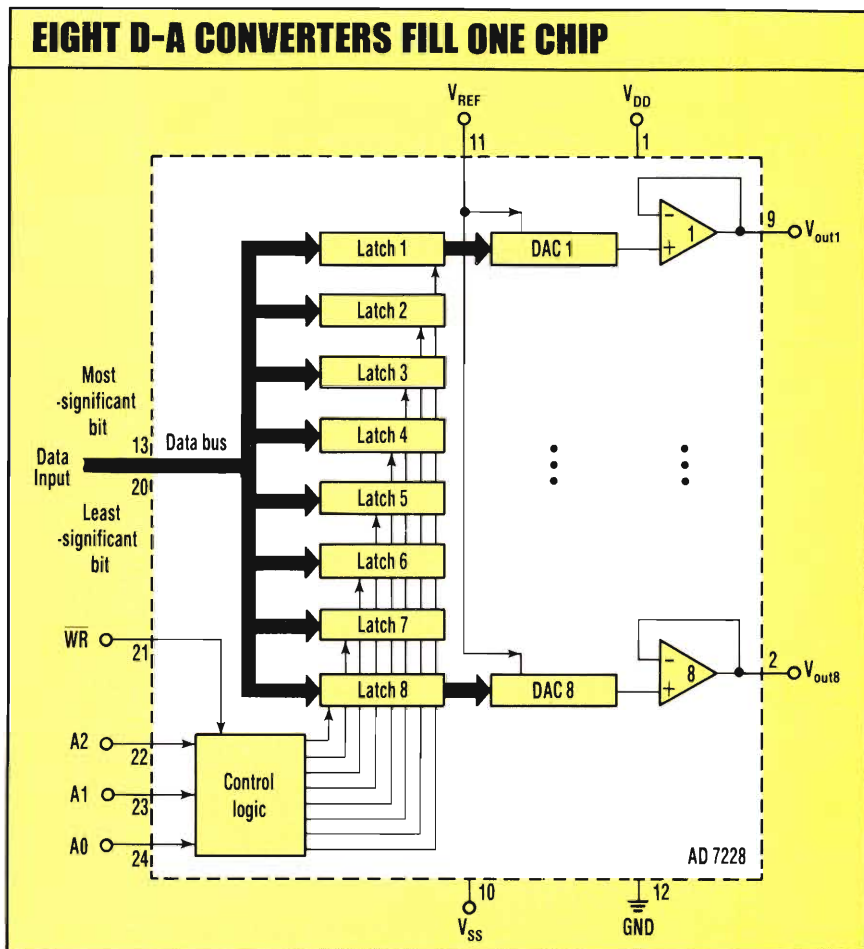
Because of its high speed and maximum propagation delay of merely 3.5 ns, the AD96687 comparator is a good choice for the application. More important than low delay, though, is propagation-delay dispersion—changes in the propagation delay from changes of input overdrive voltage. A small dispersion factor is very important in this application. The propagation-delay dispersion

2. PROGRAMMING a correction code into the eight latches included in an AD7228 for each of its d-a converters can deskew the signals to the pin drivers. A counter circuit can ramp the converter up or down to set the timing.

factor for the AD96687 is just 50 ps. Accordingly, the errors it introduces are insignificant.

For systems requiring even more accuracy and control of the program-

mable deskewing, the AD9500—a dedicated, programmable delay generator—offers a low 10-ps delay resolution with a 2.5-ns to 100- μ s-plus full-scale range. □



CIRCLE 526 MAKE LM324 OP AMP SWING RAIL TO RAIL

LEE L. STOIAN AND ROBERT A. PEASE

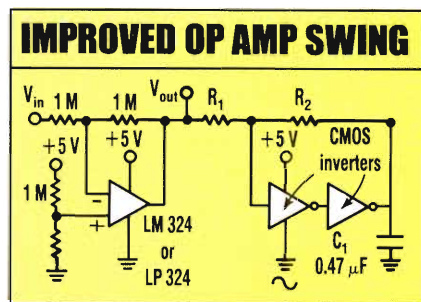
National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051; (408) 721-5000.

The popular LM324 (or LP324) op amp can operate on one 5-V supply, but its output can only swing 3 to 3.5 Vpk-pk, depending on whether the output must source current, sink current, or both. Adding two CMOS inverters (Fig. 1), however, can increase the swing from about 3.5 Vpk-pk to about 4.9 Vpk-pk (Fig. 2).

This technique is useful with sup-

ply voltages between 3 and 15 V. Just about any CMOS inverter—an MM74C00, MM74C02, MM74C14, CD4001, or CD4011—can perform this task. So can any noninverting buffer—MM74C74, MM74C86, or MM74C941—or whatever unused gates happen to be around when the project is nearly done.

But the circuit will work only for light loads of about 30 μ A and on a



1. ADDING TWO CMOS inverters can increase the op amp's output.

slow op amp like an LM324, LP324, or LM358 that has a class-B output stage. Also, whenever the CMOS inverters change polarity, the op amp's output jumps about 0.6 V for several microseconds, which obvi-

IDEAS FOR DESIGN

TYPICAL OUTPUT SWING

Op Amp	$R_1 =$	Open circuit	2.2 k	1 k	330 Ω	150 Ω
	$R_2 =$	Don't care	15 k	4.7 k	1.5 k	470 Ω
LM324	$V_{out\ Hi} =$	3.71 V	4.30 V	4.73 V	4.89 V	4.94 V
	$V_{out\ Lo} =$	0.04 V	0.023 V	0.015 V	0.010 V	0.003 V
LP324	$V_{out\ Hi} =$	4.16 V	4.91 V	4.965 V	4.982 V	4.987 V
	$V_{out\ Lo} =$	0.53 V	0.064 V	0.022 V	0.007 V	0.003 V

ously is unsuitable for precision audio preamplifiers.

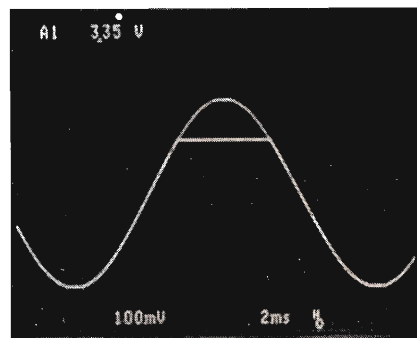
Still, for basic dc applications with light loads, the circuit's output swing compares quite favorably with a good CMOS op amp, such as the LMC660. That op amp can drive a 1-mA load closer to the rails than this circuit can drive a 30- μ A load.

Though resistor values of 150 Ω and 470 Ω for R_1 and R_2 are practical (see the table), they can be as low as 51 Ω and 330 Ω . The circuit's efficiency, though, isn't very good for those

very low values. In addition, an optional bypass capacitor C_1 in the range of 0.2 to 2.2 μ F helps cut the size of the jump and slows the response of V_{out} .

When V_{out} is between 0.1 and 2 V, the CMOS inverters are below their threshold of about +2.5 V and pull down V_{out} . This condition helps the op amp's output pull down closer to the ground. In fact, at a V_{out} of less than 0.6 V, just the CMOS circuit pulls down significantly, but only when under the control of the op

amp, which pulls up at that level. When the op amp output exceeds the threshold, as set by the ratio of R_1 and R_2 , the CMOS inverters switch state and begin pulling up on the output. Then the op amp maintains control by pulling down. \square



2. THE SWING of the op amp increased from 3.5 V pk-pk to 4.9 V pk-pk. In the circuit, the peak-to-peak output swing is determined by resistors R_1 and R_2 .

load. An FET source follower can isolate the Iso-Gate output from the large input capacitance of the MOSFET to improve the circuit's speed. Or if the application doesn't need the full 50-W load capability, the circuit can use a smaller die-sized MOSFET.

Also, the AD204 has isolated ± 7.5 -V power available on the load side for other circuitry. For instance, that power could supply an LP311 comparator on the load side to make an undervoltage-lockout or overcurrent-limit circuit. □

amount back to pin 5 reduces the gain. Even with the added op amp in the feedback path, the stability of the circuit is excellent (*Fig 2*).

To better understand the circuit's operation, consider the INA117 to be a four-input device where E_2 is the signal at pin 2; E_3 at pin 3; E_5 at pin 5; and so forth. The output voltage is: $E_0 = E_3 - E_2 + 19E_5 - 18E_1$.

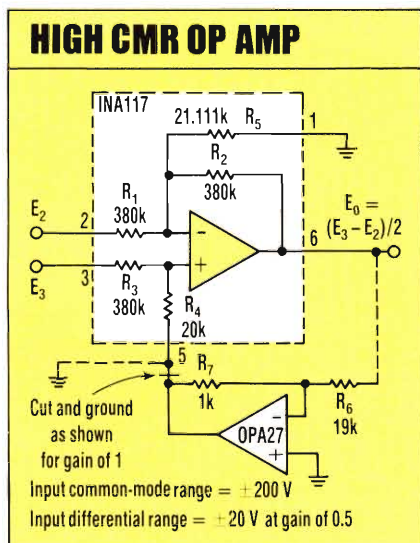
With E_1 grounded (equal to 0 V) the reduced differential gain is: $A = 1/[1+19/(R_6/R_7)]$ and for $A = 0.5$, $R_6/R_7 = 19$.

Because of the low output impedance of the OPA27 circuit, the impedance at pin 5 of the INA117 is low. Consequently, the INA117's critical resistor matching, gain, and common-mode rejection are preserved. To adjust the common-mode rejection for critical applications, add a 10- Ω fixed resistor in series with pin 5 and a 20- Ω variable resistor in series with pin 1. Short pins 2 and 3 together and drive them with a 500-Hz square wave. A square wave instead of a sine wave allows the ac signal to settle out and makes the dc CMR easier to observe on an oscilloscope and adjust. At high gain, trim the circuit to minimum output with the 20- Ω variable resistor. This trimming of the CMR may change the gain slightly. If it does, then adjust the R_6/R_7 ratio to adjust gain. This adjustment will not affect the CMR. □

CIRCLE 526 OP AMP HANDLES HIGH COMMON-MODE VOLTS

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1. THIS MONOLITHIC

difference amplifier can accept common-mode input signals as high as ± 200 V, though it operates from standard ± 15 -V power supplies.

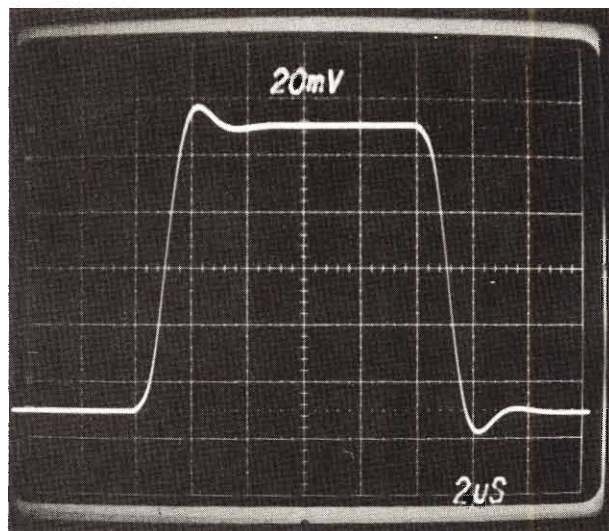
The INA117, a monolithic difference amplifier, can accept common-mode input signals to ± 200 V, though it operates from standard ± 15 -V power supplies. Many applications require an amplifier with both a high common-mode and a differential-input capability.

This high common-mode-rejection capability results from the roughly 20-to-1 resistor dividers internally supplied on the inputs of the op amp (*Fig. 1*). With that attenuation, a ± 200 -V common-mode signal reduces to ± 10 V at the op amp's two inputs. This arrangement rejects the common-mode signal, but passes dif-

ferential signals at unity gain. The proper resistors in the op-amp circuit can set the gain independently of the common-mode-rejection ability. But for the gain to remain stable with temperature changes, the ratios of R_1/R_2 and R_3/R_4 must track with ratio $R_1/(R_2$ in parallel with $R_5)$.

The circuit, however, limits the INA117's differential input range to about ± 12 V, only because it has unity gain. Its ± 15 -V power supplies limit the output swing. Reducing the gain would increase the differential input range. For example, if the gain were reduced to 0.5, that would increase the circuit's differential input range to ± 20 V.

Reducing the gain just with external resistors may seem like a simple approach, but the external op-amp (OPA27) circuit for reducing the gain is much better. It preserves the INA117's extremely precise internal-resistor matching, so the circuit's common-mode rejection and its drift with temperature remain unchanged. Furthermore, the gain-reduction produced by the external op-amp circuit improves output noise. It would remain unchanged with the simpler approach. Inverting the output with the OPA27 and feeding a small



2. EVEN WITH THE OPA27 OP-AMP

feedback circuit gain of 0.5, and 1000-pF load, the stability of the INA117 circuit is excellent.

CIRCLE 521 APPLICATIONS ABOUND FOR ALLOPHONE CIRCUIT

RICARDO JIMENEZ-GARCIA

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This allophone-generating circuit is a good way to wade into speech synthesis because it controls the most important functions of an SPO256-AL2 (IC3) speech-processor (see the figure). The circuit, a general-purpose system with many uses, vocalizes 59 allophones contained in the speech processor. After filtering and amplification, its pulse-code-modulated output can drive an 8-Ω speaker.

The processor's address pins (A₁ to A₆) define 64 speech-entry points. The address-load pin (ALD) loads the six address bits into the processor when it receives a negative-going pulse. A high-standby pin (SBY) output signal from the processor indicates to the CD4093 NAND gate (IC4) that the chip is ready for a new input command. SBY stays high until the address loads into the processor.

Closing the test switch to the NAND gate lowers its output, thereby loading an address and triggering the ALD input for an allophone cycle. SBY now goes low and stays low for an interval appropriate to that particular allophone; that is, until the chip stops vocalizing.

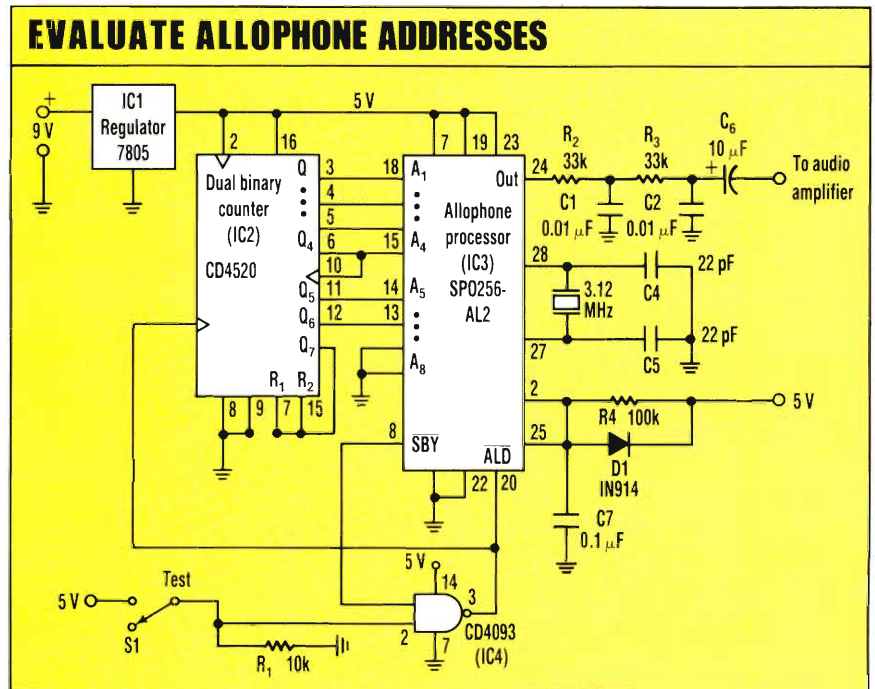
The CD4520 dual binary counter (IC2) counts from 0 to 63 in binary code until its Q₇ output resets it on the number 64 count. The NAND gate changes the state of the counter at a positive-going edge of its output pulse. Therefore, at the time that the processor starts to deliver an allophone and SBY goes low, ALD goes high to trigger the counter to deliver a new address. The new address is now ready on the processor address inputs, waiting to be loaded when ALD goes low again at the end of the vocalization period.

ALD going low also starts a new allophone cycle. In this way the circuit delivers the 59 allophones followed by 390 ms of silence, which

represent five pauses. Finally, to generate a phrase, just add an EPROM between IC2 and IC3 that

contains a program for a predetermined sequence of allophones. The EPROM outputs connect to the IC3 address input.

The circuit can serve to evaluate the latest Microchip speech narrators, SPO216 and 264, and read their word list. The SPO264, for example, contains 64 useful messages which can be played back in a female voice. □



AN ALLOPHONE GENERATING CIRCUIT controls the most important functions of an SPO256-AL2 (IC3) speech-processor.

CIRCLE 522 CROSSOVER NETWORKS ARE PHASE EQUALIZED

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When cascaded with a given low-pass network, an all-pass network of the proper order can equalize the overall phase delay over a given frequency range (Fig. 1). As a result, a crossover network free of phase-shift errors becomes possible. This equalization occurs because the compensating phase shift caused by an all-pass network of the proper order can be nearly as large as that of a

low-pass network of a given order.

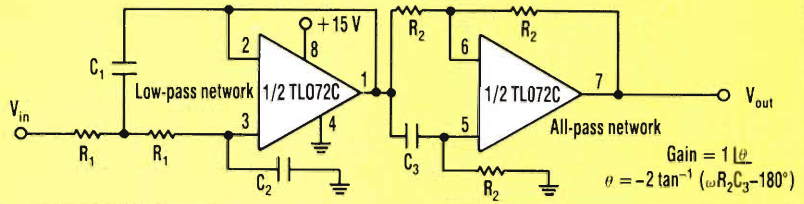
For example, consider the combination of a Butterworth low-pass filter and an equalizer. Which order is the best combination? For phase shift θ , the phase delay is $D(\omega) = -d\theta/d\omega$, where ω is $2\pi f$ and f = frequency. The effectiveness of the equalization then is $\Delta D = D(\omega_{max}) - D(\omega = 0)$, where ΔD is measured in seconds.

The computed results leads to sev-

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eral important conclusions (see the table). Two Butterworth low-pass networks of the second order in cascade, with or without an equalizer of the second order—as frequently used for crossover filters—give the same value of ΔD , about 0.585 seconds. Consequently, the all-pass network has no effect on the flatness of the phase-delay characteristics. Combining one Butterworth low-pass of the second order and one all-pass of the first order to create a

BUILDING BLOCK FILTER



1. THE BASIC BUILDING BLOCK FOR implementing a crossover filter consists of a Butterworth low-pass filter of the second order and an all-pass network of the first order. The all-pass network has little effect on phase-delay.

COMPARATIVE ANALYSIS OF FILTER TOPOLOGIES

Filter type:	Delay (D) in seconds
1. Butterworth low-pass of the 4th order	1.296503128
2. Butterworth low-pass of the 4th order plus equalizer of the first order Butterworth low-pass of the 4th order plus equalizer of the second order	0.7279840 - 0.7463950866
3. Two Butterworth low-pass networks of the second order in cascade	0.585784962
4. Two Butterworth low-pass networks of the second order in cascade with an equalizer of the second order	0.585784962
5. One Butterworth low-pass network of the second order without an equalizer	0.2928920
6. One Butterworth low-pass of the second order in cascade with an equalizer of the first order	0.0287793211

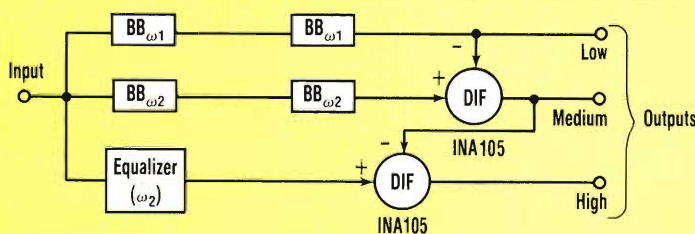
building block makes ΔD equal 0.0287 seconds. Hence, cascading two such combinations gives a total value to ΔD of just 0.058 seconds, which still is one-tenth that of the former cases.

Two cascaded building blocks, one with a low-frequency low-pass cutoff at ω_1 and the other with a medium-frequency low-pass cutoff at ω_2 , supply the low- and medium-band outputs of a crossover filter when connected in parallel through a differential-input op amp, such as an INA105 (Fig. 2). The circuit needs only an equalizer section to create the high-frequency band output. There will be little effect on phase. □

VOTE!

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BUILDING BLOCK CROSSOVER CIRCUIT



Output amplitude (dB)	Low pass	Low output band	ω_2
		Band pass	
			$\omega = 2\pi f$
	ω_1	High output band	
			Frequency (rad/s)

2. A THREE-BAND CROSSOVER FILTER uses two building-block circuits in cascade and an all-pass circuit, all paralleled through two op amps. The differential input op amp, INA105, evens out the differences in amplitude between low, medium, and high frequency bands.

Obtain accurate ratios with standard resistors

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When choosing resistor values for voltage dividers, designers usually select a convenient value for one resistor—such as 1 k Ω , 10 k Ω , and so forth—and solve for the other in terms of the required divider ratio. But that procedure typically results in a nonstandard value for the second resistor in the divider. The problem is that custom resistors with nonstandard values are expensive.

Most of the time, though, some combined standard values can supply very close to the desired ratio. With a calculator or computer program, a user can select the resistor pair to a desired degree of accuracy—standard values of 2%, 1%, and 0.1%—and avoid the cost of custom resistors. More universally applicable, though, is a comprehensive list (*see the table*).

Given are values for ratios, D , from 0.01 to 0.49, and users must supply the appropriate decade value. For values of $0.51 \leq D \leq 0.99$, merely enter the table with the value $1-D$ and reverse the values listed for R_1 and R_2 . (Of course, for $D = 0.5$, $R_1 = R_2$.)

Accordingly, if the ratio $D = 0.9$, from the ratio column on the listing at $D-1 = 0.1$ for a 2% tolerance, select from the $R_1 = 1.87$ and from the R_2 column the value for $R_2 = 16.9$. Of course, these values must be multiplied by the appropriate decade to 1.87 k Ω and 16.9 k Ω , or say, 18.7 k Ω and 169 k Ω , as required, thereby allowing the divider to draw a current level suited to the design. The usual method with standard resistor sizes would have given $R_1 = 1.0$, and $R_2 = 9.09$, the closest standard value, giving a 0.9009 ratio.

The ratios obtained with values from the table are more accurate: 0.9004 from the 2% column, 0.9003 from the 1% column, and 0.9000 (exact) from the 0.1% column.

Standard-resistor ratios						
Ratio (D)	Tolerance					
	2%		1%		0.1%	
	R_1	R_2	R_1	R_2	R_1	R_2
0.01	100.00	1.00	100.00	1.00	198.00	2.00
0.02	56.20	1.15	137.00	2.80	102.00	2.08
0.03	36.50	1.15	280.00	8.66	38.80	1.20
0.04	27.40	1.15	102.00	4.22	24.00	1.00
0.05	24.90	1.33	21.50	1.13	23.40	1.23
0.06	17.80	1.15	21.50	1.37	17.40	1.11
0.07	115.00	8.66	18.20	1.37	18.20	1.37
0.08	11.50	1.00	11.50	1.00	11.50	1.00
0.09	10.00	1.00	10.00	1.00	18.20	1.80
0.10	16.90	1.87	10.20	1.13	9.09	1.01
0.11	13.30	1.62	17.40	2.15	8.98	1.11
0.12	11.50	1.54	11.00	1.50	11.00	1.50
0.13	13.30	1.96	11.30	1.69	10.70	1.60
0.14	11.50	1.87	10.70	1.74	12.90	2.10
0.15	16.20	2.87	11.30	2.00	10.20	1.80
0.16	13.30	2.49	10.50	2.00	10.50	2.00
0.17	18.70	3.83	18.70	3.83	18.70	3.83
0.18	11.50	2.49	13.70	3.01	13.70	3.01
0.19	4.87	1.15	4.32	1.02	19.10	4.48
0.20	16.90	4.22	10.20	2.55	10.20	2.55
0.21	11.50	3.01	4.02	1.07	4.02	1.07
0.22	4.02	1.15	11.50	3.24	11.50	3.24
0.23	3.83	1.15	3.57	1.07	6.26	1.87
0.24	19.60	6.19	4.75	1.50	3.61	1.14
0.25	11.50	3.83	10.20	3.40	3.12	1.04
0.26	11.50	4.02	10.20	3.57	3.70	1.30
0.27	11.50	4.22	3.09	1.15	3.65	1.35
0.28	11.50	4.42	2.74	1.07	3.24	1.26
0.29	11.50	4.64	2.49	1.02	10.70	4.37
0.30	11.50	4.87	2.49	1.07	2.80	1.20
0.31	11.50	5.11	2.55	1.15	3.65	1.64
0.32	11.50	5.36	2.43	1.15	2.21	1.04
0.33	11.50	5.62	2.80	1.37	4.02	1.98
0.34	11.50	5.90	2.67	1.37	1.98	1.02
0.35	11.50	6.19	10.70	5.76	2.34	1.26
0.36	4.64	2.61	4.32	2.43	2.08	1.17
0.37	1.96	1.15	1.96	1.15	1.89	1.11
0.38	1.87	1.15	1.74	1.07	10.10	6.19
0.39	1.78	1.15	2.15	1.37	13.70	8.76
0.40	1.96	1.33	1.50	1.00	1.50	1.00
0.41	11.50	7.87	1.54	1.07	1.54	1.07
0.42	11.50	8.25	1.58	1.15	1.45	1.05
0.43	2.15	1.62	2.15	1.62	1.67	1.26
0.44	1.40	1.10	1.40	1.10	1.40	1.10
0.45	1.62	1.33	1.62	1.33	1.43	1.17
0.46	1.96	1.69	1.33	1.13	1.35	1.15
0.47	1.69	1.47	6.98	6.19	5.30	4.70
0.48	1.15	1.05	1.62	1.50	1.30	1.20
0.49	1.69	1.62	1.69	1.62	2.32	2.23

Tame photodiodes with op-amp bootstrap

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Applying a basic op-amp current amplifier to photodiodes presents three severe problems: high nonlinearity, oscillations, and a latch condition. All three result from the presence of load-signal voltage fed back to the photodiode. A simple bootstrapping arrangement, though, can remove them all.

In the basic circuit (see the figure, part a), two resistors, R_1 and R_2 , control the positive and negative feedback, respectively. Consequently, they also control the current amplifier's gain. All the signal current, i_p , from the photodiode flows through R_1 (negligible current flows into the op amp's input), thereby defining the input-to-output voltage drop of the op amp. Because of the op amp's very high open-loop gain and the feedback arrangement, the circuit replicates that voltage across R_2 to keep the differential voltage between the op amp inputs close to zero. As a result, feedback current i_o flows into the load Z_L through R_2 . Thus, the current gain i_o/i_p , or A_i , equals R_1/R_2 .

Because the photodiode's responsivity changes as its voltage changes with light input, variation of the voltage across Z_L , which is also across the photodiode, causes nonlinearity. Even worse, the photodiode's capacitance C_D rolls off the negative feedback from R_1 at high frequencies. Consequently, the positive feedback from R_2 can dominate, and oscillations can result. In fact, C_D inadvertently converts the circuit to a conventional op-amp square-wave generator. If large enough to stop oscillations, a dominant roll-off bypass capacitor C_B added across the load would devastate the circuit's bandwidth.

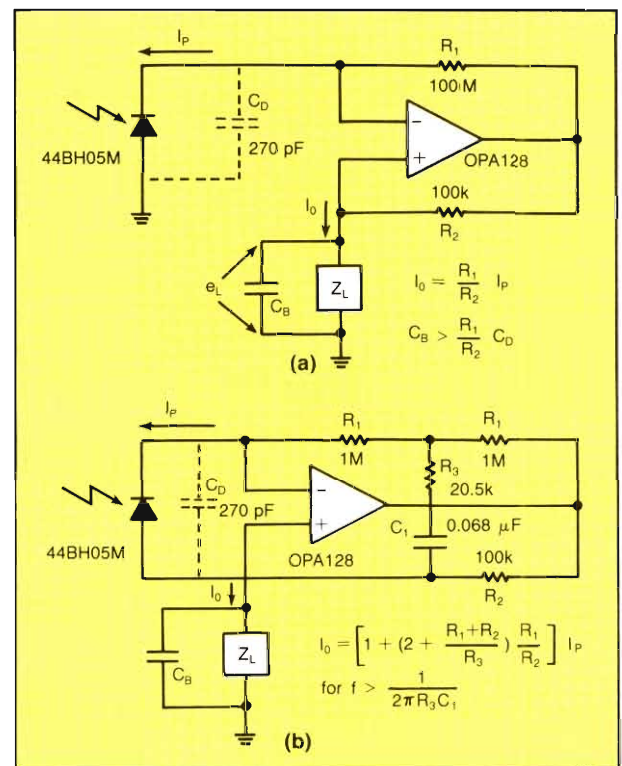
Moreover, under the condition of input overloads, which can occur during turn-on, a high impedance load could create a latch state in conjunction with the diode. If the load impedance supports a great enough voltage, positive feedback takes continuous control at the amplifier's noninverting input. At the inverting input, the photodiode clamps the voltage and prevents negative feedback recovery.

Bootstrapping, though, removes each of these problems that are caused by load voltage on the photodiode (see the figure, part b). In the new circuit, the load voltage drives the end of the photodiode that's grounded in

the basic circuit. Also, a feedback-tee circuit option becomes possible. With only the very small op-amp differential input-error signal across the photodiode, its response is essentially linear. Moreover, the canceled-out positive feedback signal on C_D avoids the square-wave generator action.

Through its effect on feedback, the bootstrapping preserves bandwidth in two ways. The negative-feedback network riding on top of the positive-feedback signal always ensures a net negative feedback. The circuit requires little if any load bypassing. As a result, this arrangement reduces the bandwidth-limiting bypassing effect of the load and its capacitance comparable to that of traditional current-to-voltage conversion circuits. Also, because positive feedback can no longer dominate, the circuit eliminates input clamping by the photodiode and the latch state.

The bootstrapping circuit also benefits from the use of a feedback tee network. In the bootstrapping circuit, the tee, like the photodiode, also rides atop the load to similarly avoid the positive-feedback effects. Tee networks offer a degree of frequency-response control. In the tee, capacitor C_1 blocks the low-frequency shunting effects of R_3 to produce a high-pass response without an amplified offset voltage.



A basic current amplifier for a photodiode (a) suffers from severe problems. A bootstrap arrangement (b) can correct them all.

stable condition in the Z80's daisy-chained interrupt priority structure, the circuit has been designed so that an interrupt status signal cannot change when the Machine Cycle 1 line, \overline{M}_1 , is low.)

An active-low interrupt request signal (\overline{INT}) from the support chip is sent to the CPU system through IC₅, an inverter, to indicate the start of the cycle. The interrupt acknowledge line (INTA) from the 8086 or 8088 system is connected to the clock inputs of dual flip-flops IC_{1A} and IC_{1B}, as well as to an OR gate, IC₃. Therefore, when the first INTA pulse ends, \overline{M}_1 goes

low. At the start of the second pulse, the I/O Request line (IORQ) also goes low. The requesting device with the highest priority is allowed to place its interrupt vector on the data bus and set an internal latch that indicates the interrupt is under service.

At the end of the second pulse, the Q₂ output from flip-flop IC_{1B} goes low, resetting IC_{1A}, as well as \overline{M}_1 and IORQ. A third flip-flop, IC_{2A}, samples the Q₂ output from IC_{1B} and resets the latter device at the end of the cycle. The length of the reset pulse is determined by the frequency of the clock used by IC_{2A}.

TI-59 program finds elliptic transfer function for low-pass filters

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J. Manuel Ramírez-Cortés

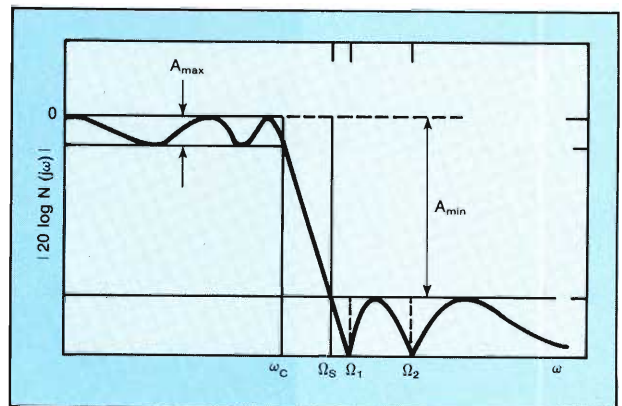
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Of all filtering functions, the elliptic transfer function is among the most useful because of its steep fall-off at the band edges (see the figure). A program designed for the TI-59 calculator can help evaluate the function by finding the odd-order poles and zeros of a low-pass filter (see the program). The algorithm calculates several things:

- The transmission zeros— ΩK , where $K = 1, 2, \dots, (N-1)/2$;
- The minimum attenuation at the stop band with respect to the maximum value at the pass band A_{\min} expressed in dB;

- The real poles (P_0);
 - The complex-conjugate poles (P_K)
- The conjugate poles are equal to $\alpha_K + j\beta_K$, where α_K is the real part and β_K is the imaginary part of the K^{th} pole.

Data supplied by the user (Table 1) includes the order of the filter (that is, the number of poles, or N); the cut-off frequency (ω_c), express-



A calculator program determines the poles and zeros of an elliptic transfer-function filter, one characterized by its steep fall-off at the band edges.

DESIGN SOLUTIONS

ed in radians/s; the stop-band frequency (Ω_s), expressed in radians/s; and either the reflection coefficient (ρ), shown as a percentage, or the maximum attenuation of the pass-band ripple in dB (A_{\max}).

The last two of those parameters are related to each other by the formula:

$$A_{\max} = -10 \log \left[1 + \left(\frac{\rho}{100} \right)^2 \right]$$

Once the poles and the zeros have been found, the transfer function, $H_{(s)}$, is found with the help of the formula:

$$H_{(s)} = \frac{(S^2 + \Omega_1^2)(S^2 + \Omega_2^2) \dots (S^2 + \Omega_{(n-1)/2}^2)}{(S + P_0)(S + P_1)(S + P_1^*) \dots (S + P_{(n-1)/2})(S + P_{(n-1)/2}^*)}$$

The results obtained with the calculator program for a normalized low-pass filter—that is, one with a ω_c of 1—compare favorably with those found in other filter tables (Table 2). Values other than unity can be used. The program, which can be recorded on a magnetic card, can evaluate the elliptic transfer filtering function up to the 21st order.

*S. Darlington, "Simple Algorithms for Elliptic Filters and Generalizations Thereof," *IEEE Transactions on Circuits and Systems*, Vol. CAS-25, No. 12, pp. 975-980, 1978.

Table 1. User instructions for low-pass elliptic transfer function

Step	Procedure	Enter	Press		Display
1	Filter order	n	A		n
2	Pass-band cut-off frequency (rad/s)	ω_c	B		ω_c
3	Stop-band frequency (rad/s)	Ω_s	C		Ω_s
4a	Either reflection coefficient (%)	ρ	D		0
4b	or passband ripple (dB)	A_{\max}	E		0
5	Compute transmission zeros, Ω_k $k = 1, 2, \dots, (n-1)/2$		R/S		Ω_k
	Repeat step 5 for each value of k until 0 appears in the display.				
6	Compute stop-band attenuation, A_{\min}		2nd	C'	A_{\min}
7	Compute real pole, P_0	0	2nd	D'	P_0
8a	Compute k^{th} pole, real part	k	2nd	D'	Re (P_k)
8b	Compute k^{th} pole, imaginary part		2nd	E'	Im (P_k)
	Repeat steps 8a and 8b for each value of k $k = 1, \dots, (n-1)/2$				

Table 2. Results of calculation for a low-pass filter

Input	Output	
	Zeros	Real and complex poles
n = 5	$\Omega_1 = 1.465436966$	$P_0 = -0.3186089933$
$\omega_c = 1$	$\Omega_2 = 1.656220908$	$P_1 = -0.2095320012 + J \quad 0.6875524703$
$\Omega_s = 1.414213562$	$\Omega_3 = 2.165997414$	$P_2 = -0.0582836518 + J \quad 0.991367843$
$\rho = 50\%$	$\Omega_4 = 3.944466518$	
	$A_{\min} = 51.4064495 \text{ dB}$	

TI-59 program for filter transfer function

000	76	LBL	065	43	RCL	130	95	=	195	04	4	260	95	=
001	11	A	066	08	08	131	39	CDS	196	04	4	261	34	FX
002	42	STD	067	91	R/S	132	55	+	197	42	STD	262	85	+
003	10	10	068	76	LBL	133	43	RCL	198	54	54	263	43	RCL
004	04	4	069	14	D	134	15	15	199	04	4	264	01	01
005	42	STD	070	55	+	135	95	=	200	42	STD	265	35	1/X
006	02	02	071	01	1	136	35	1/X	201	02	02	266	95	=
007	01	1	072	00	0	137	76	LBL	202	02	2	267	65	x
008	02	2	073	00	0	138	34	FX	203	45	YX	268	43	RCL
009	42	STD	074	95	=	139	71	SBR	204	53	(269	46	46
010	59	59	075	33	X ²	140	61	GTD	205	43	RCL	270	95	=
011	43	RCL	076	94	+/-	141	97	DSZ	206	10	10	271	71	SBR
012	10	10	077	85	+	142	02	02	207	75	-	272	24	CE
013	91	R/S	078	01	1	143	34	FX	208	01	1	273	65	x
014	76	LBL	079	95	=	144	72	ST*	209	54)	274	43	RCL
015	12	B	080	28	LDG	145	56	56	210	65	x	275	45	45
016	42	STD	081	65	x	146	35	1/X	211	43	RCL	276	95	=
017	07	07	082	01	1	147	65	x	212	15	15	277	71	SBR
018	91	R/S	083	00	0	148	43	RCL	213	45	YX	278	24	CE
019	76	LBL	084	95	=	149	09	09	214	43	RCL	279	65	x
020	13	C	085	94	+/-	150	95	=	215	10	10	280	43	RCL
021	42	STD	086	76	LBL	151	01	1	216	95	=	281	44	44
022	08	08	087	15	E	152	44	SUM	217	42	STD	282	65	x
023	55	+	088	55	+	153	57	57	218	43	43	283	02	2
024	43	RCL	089	01	1	154	01	1	219	76	LBL	284	95	=
025	07	07	090	00	0	155	44	SUM	220	22	INV	285	55	+
026	95	=	091	95	=	156	56	56	221	71	SBR	286	43	RCL
027	34	FX	092	22	INV	157	43	RCL	222	75	-	287	43	43
028	42	STD	093	28	LDG	158	57	57	223	72	ST*	288	95	=
029	11	11	094	75	-	159	32	XIT	224	54	54	289	35	1/X
030	43	RCL	095	01	1	160	43	RCL	225	32	XIT	290	71	SBR
031	08	08	096	95	=	161	10	10	226	01	1	291	24	CE
032	65	x	097	34	FX	162	22	INV	227	44	SUM	292	45	YX
033	43	RCL	098	42	STD	163	67	EQ	228	54	54	293	43	RCL
034	07	07	099	01	01	164	35	1/X	229	32	XIT	294	10	10
035	95	=	100	00	0	165	00	0	230	97	DSZ	295	35	1/X
036	34	FX	101	70	RAD	166	91	R/S	231	02	02	296	95	=
037	42	STD	102	01	1	167	76	LBL	232	22	INV	297	42	STD
038	09	09	103	06	6	168	17	B'	233	43	RCL	298	53	53
039	43	RCL	104	42	STD	169	43	RCL	234	01	01	299	43	RCL
040	11	11	105	56	56	170	10	10	235	33	X ²	300	06	06
041	76	LBL	106	00	0	171	42	STD	236	65	x	301	91	R/S
042	85	+	107	42	STD	172	03	03	237	43	RCL	302	76	LBL
043	33	X ²	108	57	57	173	01	1	238	47	47	303	19	D'
044	42	STD	109	76	LBL	174	07	7	239	45	YX	304	65	x
045	58	58	110	35	1/X	175	42	STD	240	04	4	305	89	≠
046	33	X ²	111	04	4	176	56	56	241	95	=	306	95	=
047	75	-	112	42	STD	177	76	LBL	242	85	+	307	55	+
048	01	1	113	02	02	178	45	YX	243	01	1	308	43	RCL
049	95	=	114	01	1	179	73	RC*	244	95	=	309	10	10
050	34	FX	115	04	4	180	56	56	245	35	1/X	310	95	=
051	85	+	116	42	STD	181	65	x	246	28	LDG	311	42	STD
052	43	RCL	117	48	48	182	43	RCL	247	65	x	312	02	02
053	58	58	118	43	RCL	183	09	09	248	01	1	313	00	0
054	95	=	119	57	57	184	95	=	249	00	0	314	42	STD
055	72	ST*	120	65	x	185	91	R/S	250	95	=	315	01	01
056	59	59	121	89	≠	186	02	2	251	94	+/-	316	36	PGM
057	32	XIT	122	95	=	187	44	SUM	252	42	STD	317	05	05
058	01	1	123	55	+	188	56	56	253	06	06	318	17	B'
059	44	SUM	124	53	(189	97	DSZ	254	43	RCL	319	65	x
060	59	59	125	02	2	190	03	03	255	01	01	320	43	RCL
061	32	XIT	126	65	x	191	45	YX	256	33	X ²	321	53	53
062	97	DSZ	127	43	RCL	192	91	R/S	257	35	1/X	322	95	=
063	02	02	128	10	10	193	76	LBL	258	85	+	323	42	STD
064	85	+	129	54)	194	18	C'	259	01	1	324	50	50

(continued on p. 240)

DESIGN SOLUTIONS

(continued from p. 238)

TI-59 program for filter transfer function

```
325 32 X!T      353 76 LBL      381 85 +        409 42 STD      437 22 INV
326 65 x        354 10 E'      382 01 1        410 04 04      438 44 SUM
327 43 RCL      355 43 RCL      383 95 =        411 36 PGM      439 52 52
328 53 53      356 51 51      384 34 FX       412 04 04      440 92 RTH
329 95 =        357 65 x        385 85 +        413 10 E'      441 76 LBL
330 42 STD      358 43 RCL      386 43 RCL      414 36 PGM      442 61 GTO
331 51 51      359 11 11      387 05 05      415 04 04      443 42 STD
332 05 5        360 95 =        388 95 =        416 17 B'      444 49 49
333 42 STD      361 91 R/S      389 92 RTN      417 73 RC*     445 35 1/X
334 00 00      362 76 LBL      390 76 LBL      418 52 52      446 85 +
335 01 1        363 75 -        391 54 )        419 65 x        447 43 RCL
336 05 5        364 42 STD      392 43 RCL      420 02 2        448 49 49
337 42 STD      365 55 55      393 50 50      421 95 =        449 95 =
338 52 52      366 35 1/X      394 42 STD      422 35 1/X     450 55 +
339 76 LBL      367 85 +        395 01 01      423 42 STD      451 02 2
340 53 (        368 43 RCL      396 43 RCL      424 03 03      452 95 =
341 71 SBR      369 55 55      397 51 51      425 00 0        453 55 +
342 54 )        370 95 =        398 42 STD      426 42 STD     454 73 RC*
343 97 DSZ      371 55 +        399 02 02      427 04 04      455 48 48
344 00 00      372 02 2        400 36 PGM      428 36 PGM     456 95 =
345 53 (        373 95 =        401 05 05      429 04 04      457 32 X!T
346 43 RCL      374 34 FX       402 15 E        430 13 C        458 01 1
347 50 50      375 92 RTN      403 43 RCL      431 42 STD     459 22 INV
348 65 x        376 76 LBL      404 50 50      432 50 50     460 44 SUM
349 43 RCL      377 24 CE       405 42 STD      433 32 X!T     461 48 48
350 11 11      378 42 STD      406 03 03      434 42 STD     462 32 X!T
351 95 =        379 05 05      407 43 RCL      435 51 51     463 92 RTN
352 91 R/S      380 33 X^2      408 51 51      436 01 1
```

Five-transistor amplifier boosts fast pulses into 50-Ω coaxial cable

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A simple five-transistor pulse amplifier delivers 5-V pulses into a 50-Ω load, with rise times of just 2.6 ns and fall times of 3.5 ns, matching the performance of more costly circuits containing more parts. Simply by vary-

ing the supply voltage over a range of 6 to 14 V and adjusting the circuit's off-board attenuator, the pulse amplitude can be reduced to as little as 100 mV.

The circuit (see the figure) works from dc to 50 MHz and will deliver pulses as short as 10 ns. It is driven by a TTL signal through a 740S00 quad Schottky NAND gate, IC_A through IC_D. If, however, only an ECL-level signal is available, a level translator, such as the MC10125, can be substituted for the 74S00.

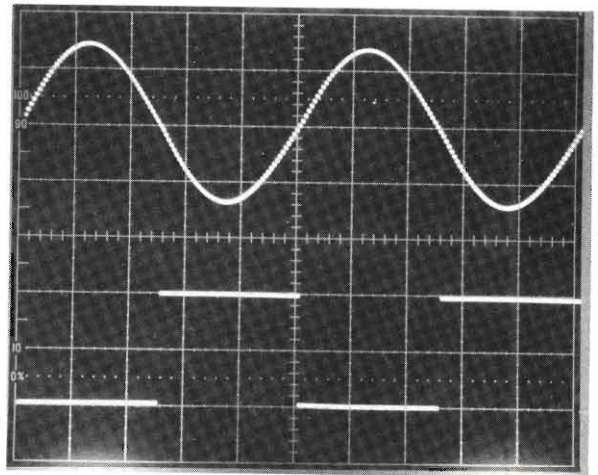
Transistor Q₁, wired as a common-emitter

clock-to-center-frequency ratio of 100:1, accomplished by tying its pin 12 to a middle supply voltage level. (A 50:1 ratio is available by tying the pin high.)

The output also drives a 100:1 CMOS divider that produces a symmetrical 1-kHz square wave. That signal is fed to the filter through resistors R_4 and R_5 .

The filter is in its bandpass, or 1a, mode and delivers its output from pin 19. Two resistors, R_2 and R_3 , control the gain and Q . An analog path to ground is furnished by a resistive divider, formed by R_6 and R_7 , which is bypassed by capacitor C_3 .

The circuit's strength is not in its overall dynamic range or signal purity but rather in its easy tunability and freedom from bouncing and uncertain settling time. Programming can be both fast and precise, the latter due in part to the v-f converter's good linearity. At an output level of 1 to 2 V rms, total harmonic distortion is on the order of 2%, limited by the clock noise.



2. The sine-wave output, shown at 1 V/division (top), exhibits just 2% total harmonic distortion (THD) for a square-wave input of one-hundredth the clock frequency, shown at 5 V/division (bottom). The horizontal scale is 200 μ s/division.

Pseudo-sine-wave circuit generates FSK tones without discontinuities

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A circuit that combines a crystal oscillator, a digital divider, and a shift register generates audio frequency-shift-keying (FSK) signals with the unusual combination of crystal-controlled accuracy and continuous-phase switching.

The common methods for generating audio-frequency signals fall short of fully achieving that objective. For instance, in the quest for

high precision, when a variable modulus counter is hooked to a crystal-controlled oscillator to switch among various audio tones, the price of precision is phase discontinuities whenever the frequency is changed. One result is that the FSK signal takes excessive bandwidth.

The usual alternative, which ensures smooth keying, is to switch an audio generator's timing components—resistors and capacitors. The problem here is frequency inaccuracy, aggravated by aging and temperature drift. In addition, the high-frequency aspects of glitches caused by the switching can increase the required transmission bandwidth and play havoc with phase-locked-loop FSK demodulators.

The combined circuit (see the figure) uses two

DESIGN SOLUTIONS

74C193 4-bit counters, IC₂ and IC₃, to divide the output of the crystal oscillator by any integer between 1 and 255. The output of the counters is applied to IC₄, a 4015B dual 4-bit shift register connected as a twisted ring counter. The various outputs of the shift register are combined, through a precision resistor network, to produce a pseudosinusoid whose frequency is $1/16$ of the input frequency, and which is a stair-step approximation of a sinusoid with 16 discontinuities per period.

With 1% precision resistors, the circuit's even-order harmonic output is too low to be measured. Odd-order harmonics—from 3 to 13—are suppressed by at least 30 dB. The 15th and 17th harmonics, generated by the stair-step discontinuities, are about 15 dB below the fundamental. If they become a problem, they can be handled easily by a low-pass filter.

Although a crystal oscillator is shown, any square-wave source is suitable. However, for reliable performance, the frequency of either should be between 1 and 2 MHz. The crystal frequency is based on the desired output. The latter is equal to the crystal frequency divided by

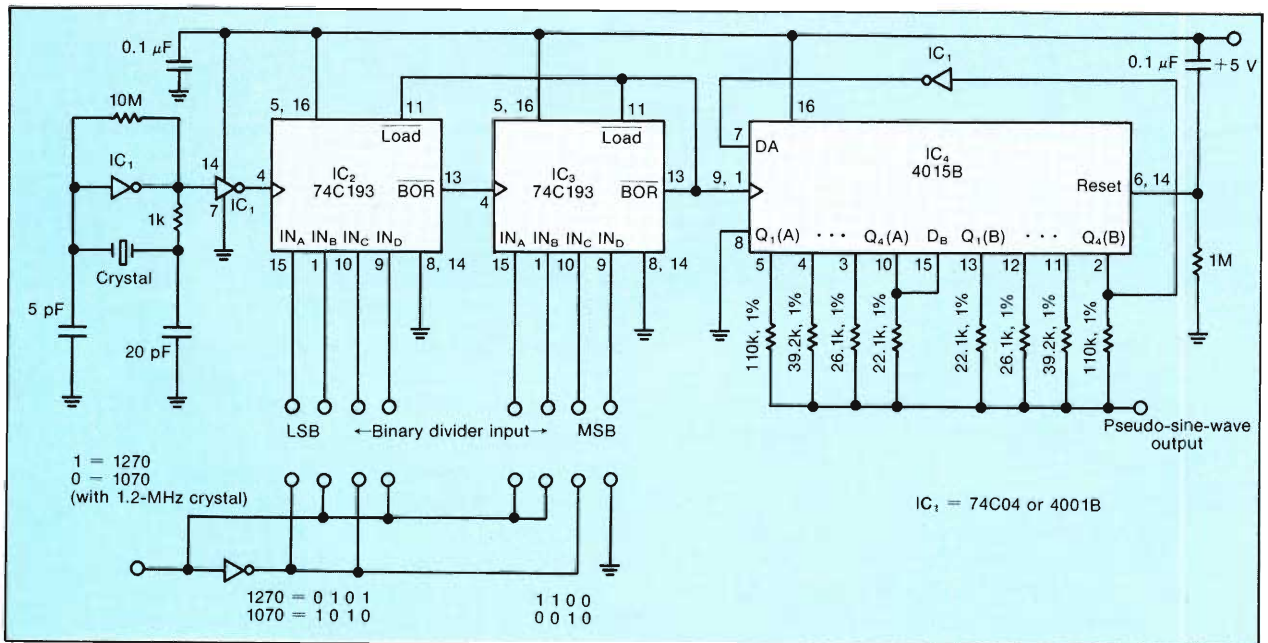
$16(N+1)$, where N is the binary input to the dividers. For example, a 1.2-MHz crystal will generate FSK frequencies of 1070 and 1270 Hz, since it gives near-integer values for the divisor N. From the formula, the values are 69 and 58 (01000101 and 00111010) respectively. The insert shows the appropriate wiring for the dividers' inputs.

Because it is a CMOS device, the shift register's output will drive the resistive combining network with a rail-to-rail swing. The pseudosinusoid will swing from ground to +5 V and the output will exhibit an impedance of approximately 4200 Ω . Although 1% resistors are shown, the nearest 5% values can be substituted if more even-order harmonic content can be tolerated.

Winner for October 4, 1984

PROM and octal latch make a simple, versatile 7-bit counter

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A useful adaptation of two rather common circuits switches between two or more sinusoidal frequencies without any abrupt phase variations.

V-f converter doubles as clock and input of stable sine-wave source

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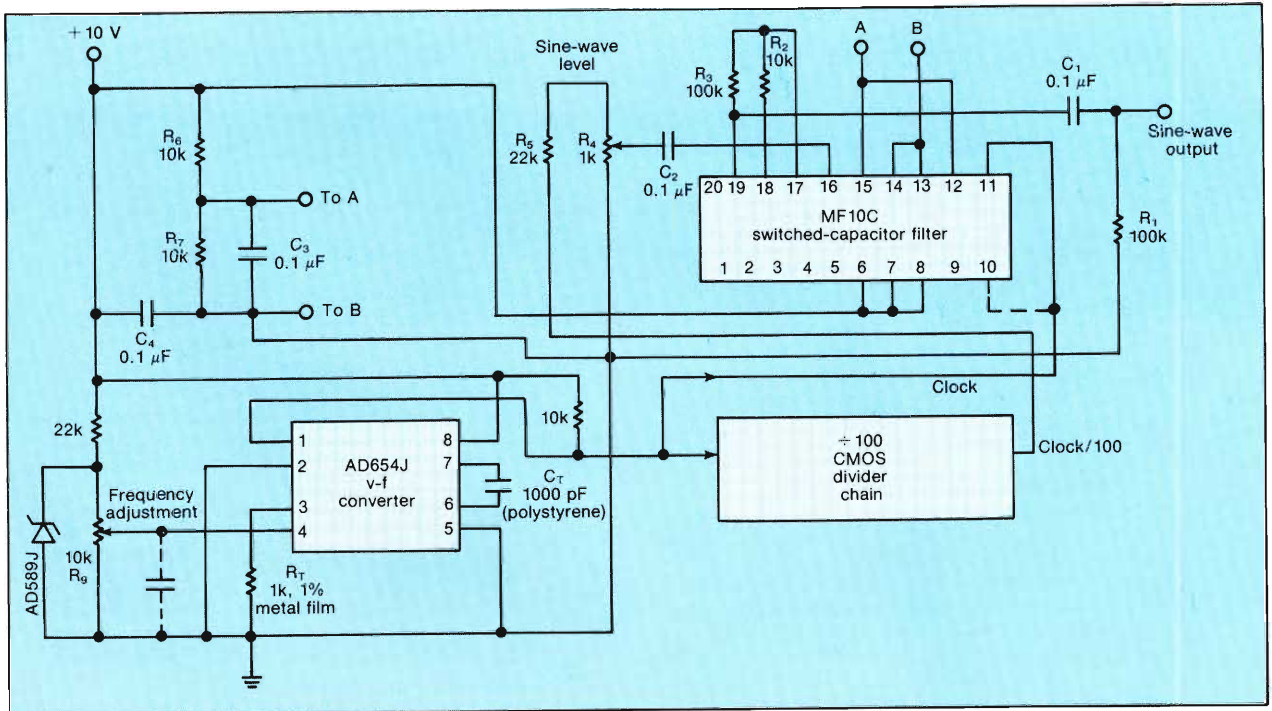
A voltage-to-frequency converter makes a versatile clock source for a switched-capacitor filter, such as the MF10C, but it can be even more valuable if its output serves as both the signal source and the clock. Such a combination of converter and filter makes a frequency-agile sine-wave source that has a very precise and predictable output.

In the circuit (see the figure), the AD654J v-f

converter operates from a single supply and has a square-wave output of up to 500 kHz. That output directly becomes the filter's clock input and is also divided down by a factor of 100 to form the filter's signal input.

The frequency of the v-f converter, here 100 kHz, is determined by resistor R_T , capacitor C_T , and the applied 1-V control voltage. The voltage is set by R_9 , a 10-k Ω potentiometer, and is stabilized against changes in the supply voltage via a 1.235 band-gap reference diode, an AD589J.

With a 10-V supply, the v-f converter produces a 10-V pk-pk square-wave output, which drives the filter. Here that filter is set to a



1. A v-f converter, the AD654J, acts as both the signal input and the clock for a switched-capacitor band-pass filter. The resultant circuit is a frequency-agile and easily programmed sine-wave source that features precise and automatic tracking.

DESIGN SOLUTIONS

Simple program finds parts values for phase-locked loop

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Phase-locked loops are among the most common and valuable system elements, and desktop computers are now making short shrift of the sometimes difficult and tedious task of designing and analyzing them. An interactive program for the HP 9825 computer (see the program listing) helps the designer determine the best component values for a given PLL filter and then guides him to the closest standard component values.

In a typical second-order PLL (Fig. 1), the phase detector and the voltage-controlled oscil-

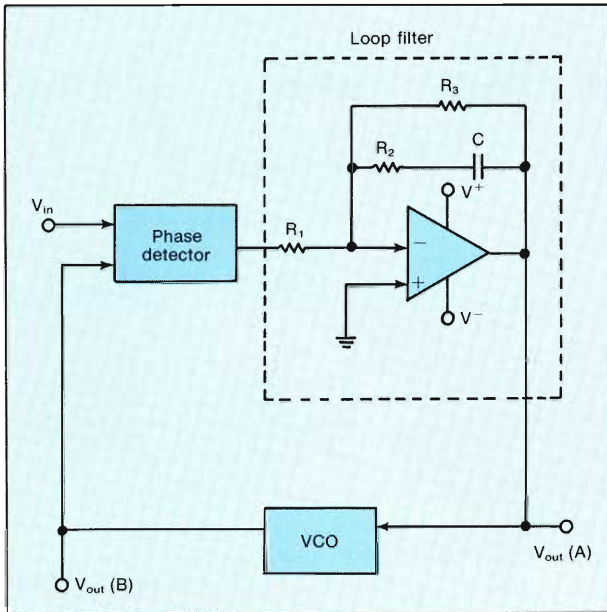
lator are selected to satisfy individual design criteria. However, the resistor and capacitor values must be determined by an algorithm based on equations described by Floyd Gardner in his book *Phaselock Techniques*.^{*} The algorithm, represented by a Werner-Orr chart (Fig. 2), is suitable only when phase-detector and VCO transfer gains can be measured independently of loop gain.

The algorithm draws on such data as the 3-dB bandwidth of the loop in hertz (Fb), the damping factor of the loop (d), the phase-detector transfer gain in V/rad (Kd), and the VCO transfer gain in (rad/s)/V. The value of resistor R₁ is an independent variable within the program.

^{*}Floyd Gardner, *Phaselock Techniques*, 2nd ed. (New York: John Wiley & Sons, 1979).

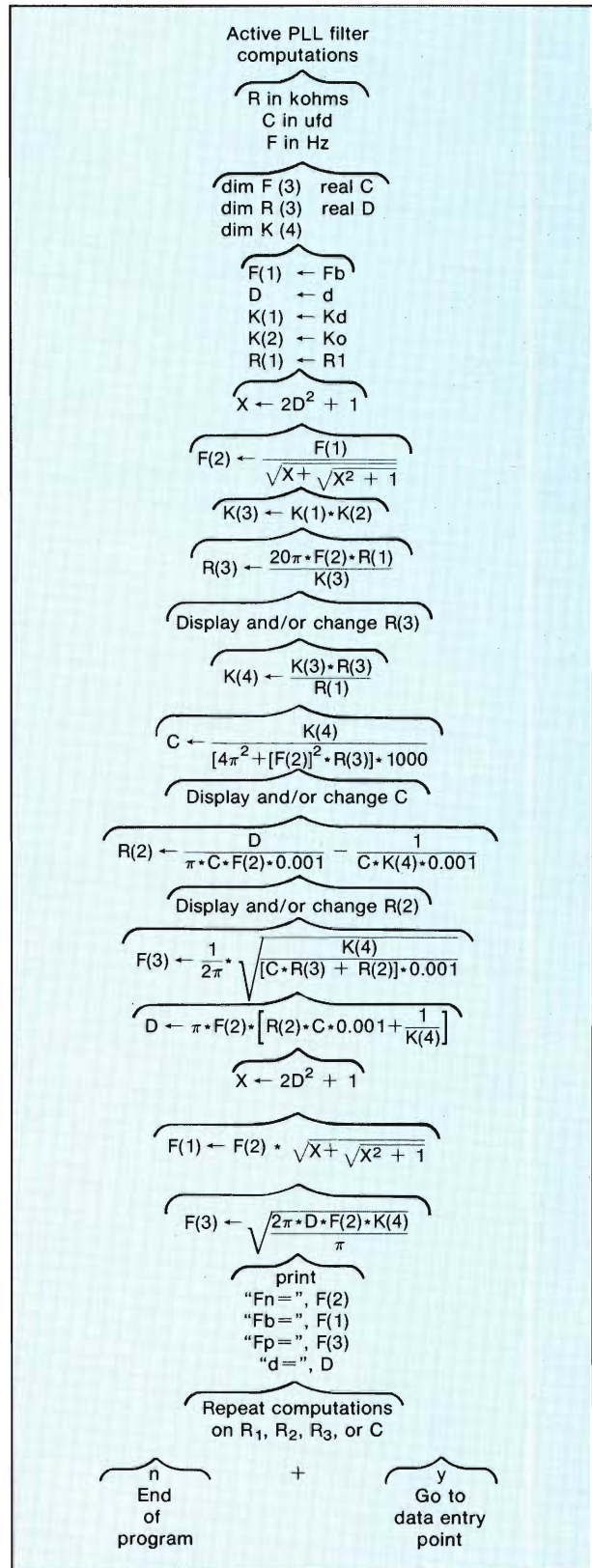
Designing an active PLL filter

```
0: dsp "ACTIVE PLL FILTER COMPUTATIONS"
1: prt "ACTIVE PLL"
2: prt "FILTER"
3: prt "COMPUTATIONS"
4: prt "*****"
5: prt "R in kohms", "C in ufd", "Frequency in Hz";spc;wait 4000
6: dim F(5); dim R(5); dim K(5); dim A$(5)
7: dsp "PLEASE SPECIFY THE FOLLOWING. . ."; wait 3000
8: ent "3db BANDWIDTH Fb(Hz)?", F (1)
9: prt "*3dB BW", " Fb=", F(1)
10: ent "*DAMPING", D
11: prt "*DAMPING", D
12: ent "PHASE DETECTOR GAIN", K(1)
13: prt "*PHASE DETECTOR GAIN", " Kd=", K(1)
14: ent "VCO GAIN", K(2)
15: prt "*VCO GAIN", K(2)
16: ent "INPUT R1(kohms)", R(1)
17: prt "*INPUT R", " R1=", R(1)
18: 2*D↑2 + 1→X
19: F(1)/√(X + √(X↑2 + 1))→F(2)
20: K(1)*K(2)→K(3)
21: 20*π*F(2)*R(1)/K(3)→R(3)
22: dsp "R3(approx.)=", R(3);wait 5000
23: prt "R3(approx.)=", R(3)
24: ent "ADJUST R3?", R(3)
25: prt "*ADJUSTED R3", " R3=",R(3);spc
26: K(3)*R(3)/R(1)→K(4)
27: K(4)/(4*π↑2*F(2)↑2*R(3))*1000→C
28: fxd 4
29: dsp "(approx.)=",C;wait 500
30: prt "C(approx.)=",C
31: ent "ADJUST C?",C
32: prt "*ADJUSTED C", " C=", C;spc
33: fxd 2
34: D/(C*π*F(2)*0.001)-1/(C*K(4)*0.001)→R(2)
35: dsp "R2(approx.)=",R(2); wait 5000
36: prt "R2(approx.)=",R(2)
37: ent "ADJUST R2?", R(2)
38: prt "ADJUSTED R2", " R2=",R(2);spc
39: prt "NEW PARAMETERS";spc
40: 1/(2*π)*√(K(4)/(C*R(3) + R(2))*0.001)→F(3)
41: π*F(2)*(R(2)*C*0.001 + 1/K(4))→D
42: 2*D↑2 + 1→X
43: F(2)*√(X + √(X↑2 + 1))→F(1)
44: √(D*2*π*F(2)*K(4))/π→F(3)
45: π*F(2)*(D + 1/(4*D))→N
46: prt "Fn=",F(2), "Fb=",F(1), "Fp=", F(3), "NB=", N, "d=", D
47: ent "REPEAT COMP. ON R1, R2, R3, C (y or n)?", A$
48: if A$="y";spc;prt "NEW CALCULATIONS OF R1, R2, R3, C";spc;gto 16
49: spc 3;end
```



1. Passive components can tailor the operation of a phase-locked loop to a specific purpose. The user must select the phase detector and VCO based on design needs; the program finds the resistor and capacitor values that best meet the design objectives. Depending on the function of the circuit, the output can be taken from either $V_{out}(A)$ or $V_{out}(B)$.

2. The algorithm that determines PLL resistor and capacitor values is visualized through a Werner-Orr diagram. The standard equations need such data as the loop's desired 3-dB bandwidth and the phase-detector and VCO transfer gains.



Isolation amp drifts ± 5 mV over 8 hours

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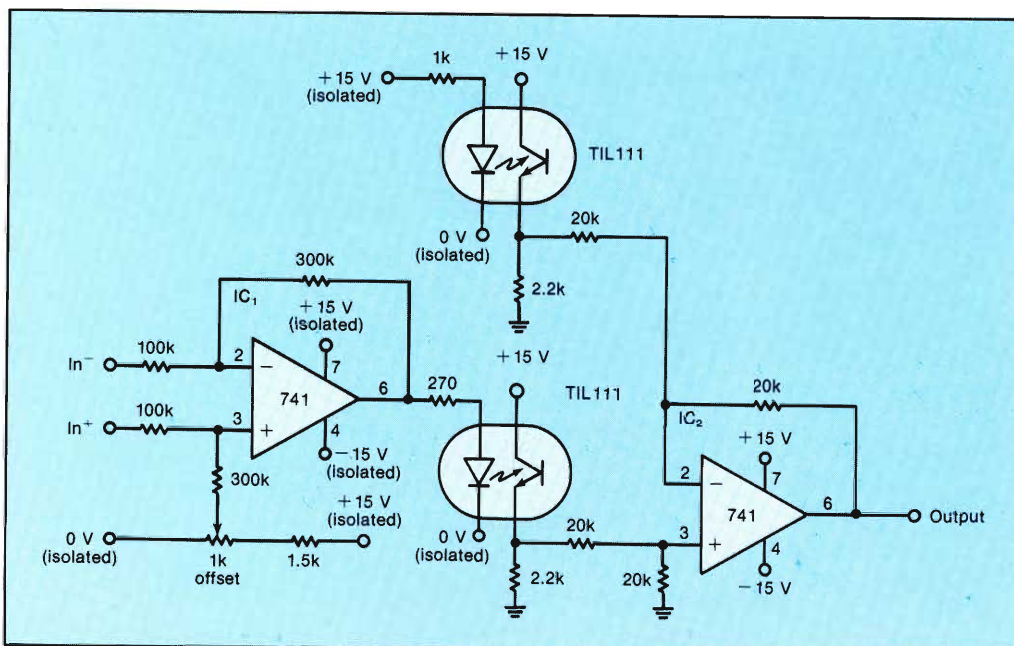
By employing two identical opto-isolators, a dc-coupled analog amplifier not only provides good input-output isolation, but also keeps its output voltage drift to no more than ± 5 mV after 8 hours at 25°C. Thermal drift in one of the circuit's two optocouplers is compensated for by similar thermal drift in the second.

The amplifier handles signals over a range of dc to 50 kHz and exhibits 1% linearity within its ± 4 -V output range. In operation, its input operational amplifier, IC₁, drives one of the two

matched optocouplers. To ensure proper linearity, the LEDs in both couplers are forward-biased so that they each conduct about 14 mA when no signal is present. A dc-offset potentiometer provides bias voltage to IC₁ in order to equalize the outputs from the optocouplers.

The emitters of the phototransistors are connected to the differential inputs of a second op amp, IC₂, which has a voltage gain of six. By use of different feedback resistors, the circuit's gain can be changed. However, to maintain a high ratio of output signal to output drift voltage, the output level of the optocouplers should be kept relatively high.

For proper circuit operation, the input operational amplifier and the photodiodes must be powered by an isolated supply. A grounded source is suitable for the phototransistors and the output amplifier.



The two identical opto-isolators in this dc-coupled amplifier negate each other's drift, keeping the circuit's output voltage stable over extended periods. The amplifier handles signals to 50 kHz and delivers a ± 4 -V output.

DESIGN SOLUTIONS

16-kbit NMOS PROM such as the 2716 has a 350-ns access. A 10-ns bipolar device can considerably increase the counter's speed.

The counter is reset by applying a pulse on the Reset line for a period longer than one clock

pulse. The address to the PROM will then come from IC₃, rather than from the PROM's output. The circuit will also reset for the next incoming clock pulse if data from the PROM matches the address set at IC₃.

Programming data for counterless counter					
State	Counter output required Q ₀	PROM address A ₀	PROM data to be burned	Control bit D ₀	Remarks
1	000 0000	0000 0000	0000 000	1	
2	000 0010	0000 0001	0000 010	1	
3	000 0001	0000 0101	0000 001	1	
4	000 0011	0000 0011	0000 011	1	
5	000 0010	0000 0111	0000 010	0	States 2 and 5 are the same
6	000 0100	0000 0100	0000 100	1	
7	000 0011	0000 1001	0000 011	0	States 4 and 7 are the same
8	000 0101	0000 0110	0000 101	1	
9	000 0100	0000 1011	0000 100	0	States 6 and 9 are the same
10	000 0110	0000 1000	0000 110	1	
11	000 0101	0000 1101	0000 101	0	
12	000 0111	0000 1010	0000 111	1	
13	000 0110	0000 1111	0000 110	0	States 10 and 13 are the same
14	000 1000	0000 1100	0001 000	1	
15	000 0111	0001 0001	0000 111	0	States 12 and 15 are the same
16	000 1001	0000 1110	0001 001	1	
17	000 1000	0001 0011	0001 000	0	States 14 and 17 are the same
18	000 1010	0001 0000	0001 010	1	
19	000 1001	0001 0101	0001 001	0	States 16 and 19 are the same

V-f converter offers 120-dB dynamic range

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Although it is built with several discrete devices, a voltage-to-frequency converter offers a wider dynamic range—120 dB—than monolithic devices. The circuit

offers an output of 1 Hz to 1 MHz for a 0-to-10-V input. The circuit's operation hinges on a control loop that uses the output frequency to balance the input current.

Op amp IC₁ integrates a positive input voltage in a negative direction. When its output crosses zero, the output of op amp IC₂ switches low. That causes the diode bridge, built around a 2.5-V reference, to limit at -3.7 V (the reference minus the forward voltage). As a result, a

initiation and the latter because of the post-test structure of the DO loop used to calculate all other powers of X. For powers of X greater than 1, the word multiplies X by itself N times.

The LEN definition assumes that a string is ended by the null character $\emptyset\emptyset H$. It counts from the beginning of the string specified by the value on the top of the stack to the character.

Wide-range oscillator operates above 20 MHz

Einar Abell

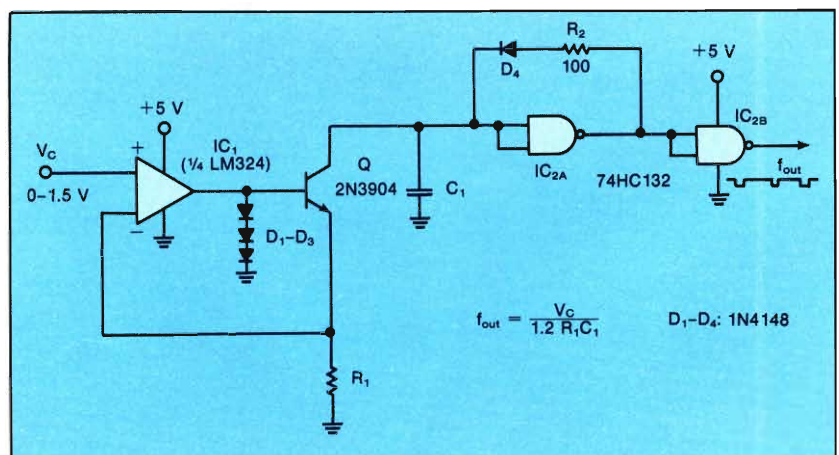
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The addition of several components to an HCMOS Schmitt trigger creates a voltage-controlled oscillator with a sweeping range of greater than 100,000:1 and an upper limit in excess of 20 MHz. The circuit is especially well suited to building frequency synthesizers that employ a phase-locked loop.

The circuit (see the figure) replaces single-chip designs that have a control range of more than 1000:1 but that cannot work above a few megahertz. Circuits that work at higher frequencies have a restricted range.

Circuit operation is simple: When the output of NAND gate IC_{2A} is high, capacitor C_1 charges rapidly through diode D_4 and resistor R_2 until the upper threshold is reached. Then, the gate's output goes low. Also, C_1 discharges to the low threshold by passing its current through a sink formed by transistor Q , resistor R_1 , and op amp IC_1 . That action creates a series of pulses whose spacing is a function of the input voltage, V_C . Diodes D_1 to D_3 clamp the voltage across R_1 to less than 1.5 V, since oscillation would cease if IC_2 's lower threshold were exceeded.

The oscillation frequency can be calculated fairly accurately if it is considered the inverse of the discharge time of C_1 . Thus starting with the formula $dV/dt = I/C$ and substituting V_C/R_1 for I and 1.2 (the difference between the upper and lower thresholds) for dV , the output



A simple voltage-controlled oscillator, built around a high-speed HCMOS Schmitt trigger, furnishes a very wide sweep range—more than 100,000:1—and an upper limit of greater than 20 MHz.

frequency becomes $f_{out} = V_C / 1.2R_1C_1$.

The circuit's operation is linear to within 1% for a V_C of less than 0.1 V. Nonlinearity increases to about 20% at 1 V, since the charge time of C_1 becomes an increasing portion of the total oscillation cycle. Another limiting factor is the delay time of the Schmitt trigger, which holds the frequency to below 30 MHz.

The op amp's positive offset can prove troublesome since the voltage across R_1 never drops to zero, thus reducing the frequency sweep to as few as two decades. The problem can be solved by an op amp with a negative offset or one that can have its offset driven negative or trimmed to zero if the output frequency must be zero for a 0-V input.

Tone-ringer circuit drives telephone-signal counter

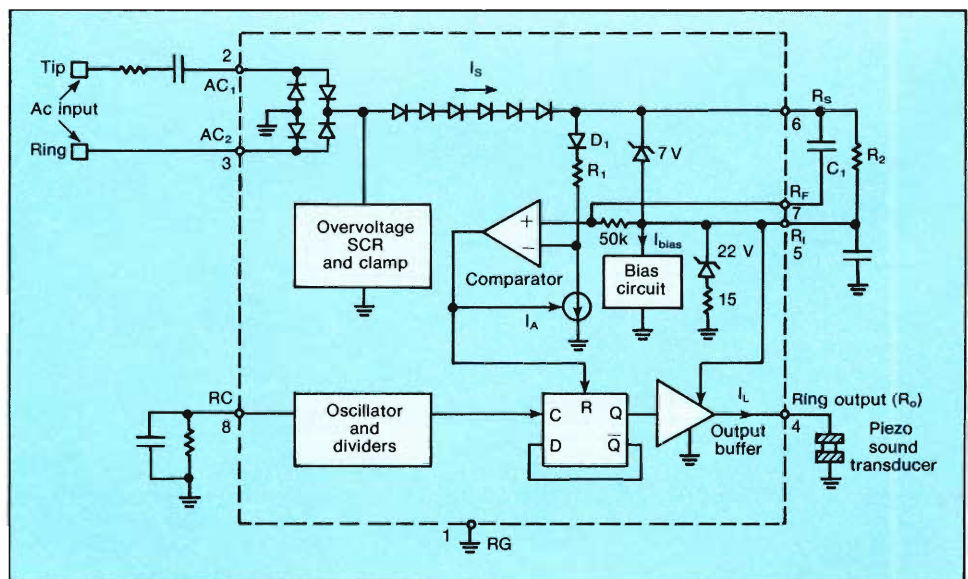
Dennis Morgan

Applications Engineer
Motorola Inc.
Semiconductor Products Sector
7402 S. Price Road
Tempe, Ariz. 85283

Although it was developed to replace bulky electromechanical bell assemblies in conventional telephone sets, the MC34012 electronic tone ringer does a good job

connecting a telephone line to a sequential ring-signal counter. The counter not only sounds a piezoelectric transducer after a selectable number of ringing pulses, it also has an auxiliary output that can turn on a variety of accessories, such as a modem or an answering machine.

In the tone ringer (Fig. 1), a full-wave bridge rectifies a ringing voltage and passes it through a string of diodes that provide the high input impedance required by telephone systems at low voltages. A small portion of the current



1. A comparator in the MC34012 tone ringer connects an oscillator to a piezoelectric transducer after detecting the incoming ringing voltage.

Precision voltage to single-ended current source sidesteps CMRR problems

D. Baert, H. Simoens and H. Kuyken

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Sint-Pietersnieuwstraat 41
B-9000 Ghent, Belgium

The Howland current pump solves some problems encountered in circuits requiring a source that can be connected with a common-ground output. But that type of op amp circuit introduces problems of its own, such as instability and a problematical input impedance, making the circuit shown in the figure a better choice.

In this circuit, two op amps, IC_1 and IC_{2A} , are connected in a follower configuration to create a high-input impedance. Eliminating the resistor bridge of the Howland source produces a better common-mode rejection ratio and lowers the output impedance. The current generated by the pair through resistor R_1 is equal to $(V_1 - V_2)/R_1$.

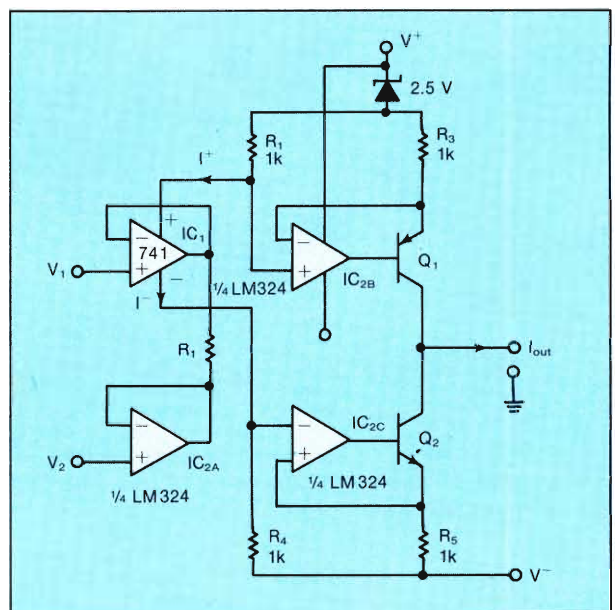
A second set of op amps, IC_{2B} and IC_{2C} , in combination with two high-frequency transistors, Q_1 and Q_2 , form precision current mirrors that are driven by I^+ and I^- , the supply currents of IC_1 . The output impedances of both mirrors are very high, since Q_1 and Q_2 operate in a common-base configuration, but they are not influenced by the relative value of the current resistors, R_2 through R_5 . The output now becomes $I_{out} = I^+ - I^- = (V_1 - V_2)/R$.

The Zener diode helps keep the circuit within the common-mode range of the LM324. But because of the good separation between the amplifier and the load impedance, high-frequency instability is not a problem.

The circuit's performance hinges on the use of 1% resistors in the current mirror. If the parts are not matched, the output current will

be offset. But if the circuit is set up properly, nonlinearity will be held to less than 0.1%. Loading the output with 2 k Ω or short circuiting it results in a change of just 0.05%. Even heating the LM324 with a soldering iron causes a minor change—about 0.1% of full scale.

Some changes can improve the circuit. For example, the transistors can be replaced with FETs to eliminate the effects of a bipolar transistor's forward current transfer ratio (h_{fe}), but the output voltage swing will be smaller. A physical change—using a network for R_2 through R_5 —can ensure more closely matched resistors as well as save board space. Also, one op amp in the package is free, it can be used to convert the output current into a voltage.



This current source, with two op amps in a follower configuration, gives good CMRR performance.

DESIGN SOLUTION

Varactor diodes lower the chip count of digital PLLs

Ronald H. Hill

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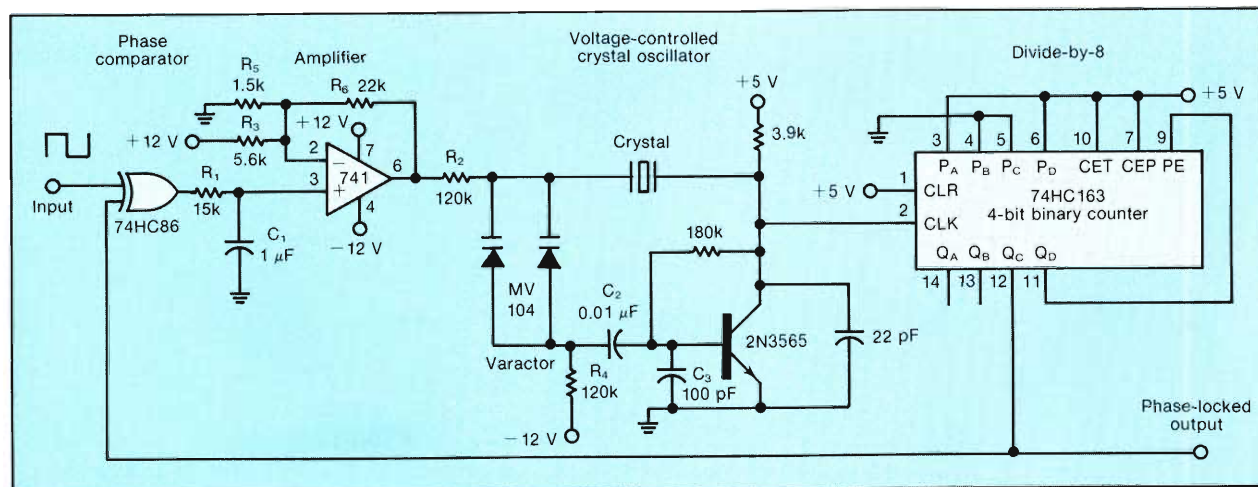
A crystal-controlled phase-locked loop is a must for low error rates in systems that recover Manchester-encoded data from transmission paths with low signal-to-noise ratios, and such loops are usually digital. A typical digital PLL could use as many as eight ICs, but just three chips will do in a circuit that uses varactor diodes to phase-lock the crystal itself.

In the circuit, a 74HC86 exclusive-OR gate compares the phase of the input signal with the phase derived from the crystal through the 4-bit binary counter (see the figure). The filter formed by resistor R_1 and capacitor C_1 smoothes the output of the gate before it is amplified by the 741 op amp.

The output of the 741 varies the voltage on two MV104 varactors, changing the diodes' capacitance and hence the crystal's frequency. Resistors R_2 and R_4 reverse-bias the diodes, and capacitor C_2 decouples their outputs.

Here, the 4-bit counter, a 74HC163, serves as a divide-by-8 circuit. However, any division factor is suitable, provided that the crystal frequency is N times the input frequency.

The 20-V control range of the varactors will produce a change in oscillator frequency of 65 ppm and a phase change of 45° between the circuit's input and output. The phase change is also inversely related to the amplifier gain, which is set by the values of resistors R_3 , R_5 , and R_6 . In addition, R_3 determines the amplifier's offset control voltage, which in this case is 0 V for an input of +2.5 V at the op amp's noninverting input. At that control voltage, the oscillator frequency will be 30 ppm above the nominal value of the crystal.



A simple three-chip digital phase-locked loop employs varactor diodes to control crystal frequency. Over a 20-V varactor voltage range, the circuit's input-to-output phase changes by 45° .

IdeasForDesign

Zero-biased photodiode rejects digital noise

In a low-noise environment, measuring low-level visible light (1 to 10 ft-cd with 0.1 ft-cd resolution) is not an especially difficult task. However, in a digital control system, with its switching noise and oftentimes less than well-regulated power supplies, the task becomes considerably more difficult. But by taking advantage of the zero-bias requirements of a blue-enhanced photodiode, noise and other forms of power supply variation can be made to appear as common-mode signals and will not disturb the performance of the detection circuit.

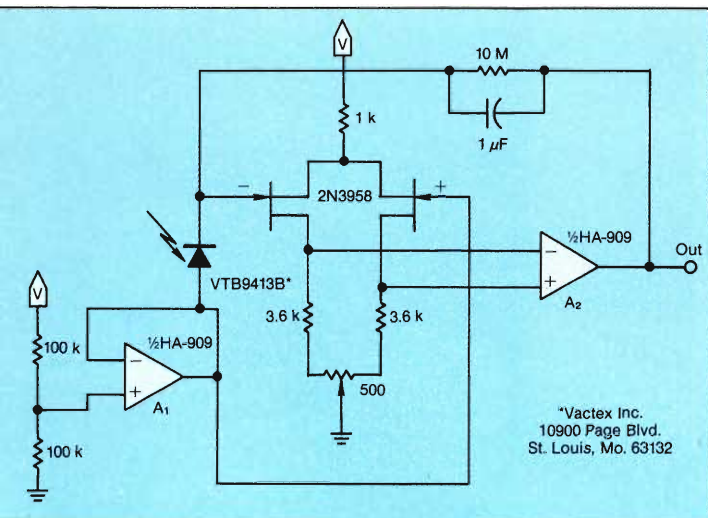
The zero-bias scheme shown in the figure allows the photodiode, a VTB9413B, to operate as a pure current source, virtually eliminating shunt resistance leakage, a cause of offset errors. Op amp A_1 serves as a voltage follower reference and puts the same potential at the positive gate of the dual FET that it places at the cathode side of the photodiode. Op amp A_2 senses the difference in source voltage

between the two FETs and puts out a correcting voltage to the negative end of the dual FET. Because that end is enclosed within the feedback loop of A_2 , the voltage at both gates will be equal, thus maintaining zero bias across the photodiode.

In addition to the noise-canceling effects of the zero-bias arrangement, the amps' supply-voltage rejection ratio tends to limit variations that would decrease overall circuit noise immunity. Ground noise, too, is rejected by A_1 , as well as by the inherent characteristics of the matched FETs.

The photodiode produces $0.013 \mu\text{A}/\text{ft-cd}$ across the visible light range. Tests indicate that the circuit will have less than 1% change in output for a supply voltage change of up to 3 V peak to peak. The bandwidth is about 200 Hz when a 5-ft-cd LED source is closely coupled to the photodiode.

Richard Persh, 8352 Shady Grove Circle, Manassas, Va. 22110.



Winner for March 17, 1983

"LED switching driver cuts current draw to 3 mA"

Ralph J. Ursoleo, Electronics Engineer, Physics Electronics Shop, University of California, Santa Clara, Calif. 93106.

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A zero-biasing scheme makes this photodiode circuit relatively immune to the effects of digital switching noise and power supply variations. The inherent voltage regulation characteristics of the op amps also help improve the reliability of low-light-level readings in a noisy environment.

Bootstrapped analog switch cuts harmonic distortion

A bootstrapped circuit that operates like an automatic gain control circuit reduces the harmonic distortion caused when analog signals pass through CMOS analog switches. The circuit, shown in Fig. 1, eliminates the nonlinear relationship between the signal voltage and switch resistance when the switch is turned on.

The usual method for reducing the effect of signal-dependent on-resistance is to have the switch work into a high-impedance load. In that case, the change in switch resistance with a varying signal voltage becomes a small percentage of the total resistance.

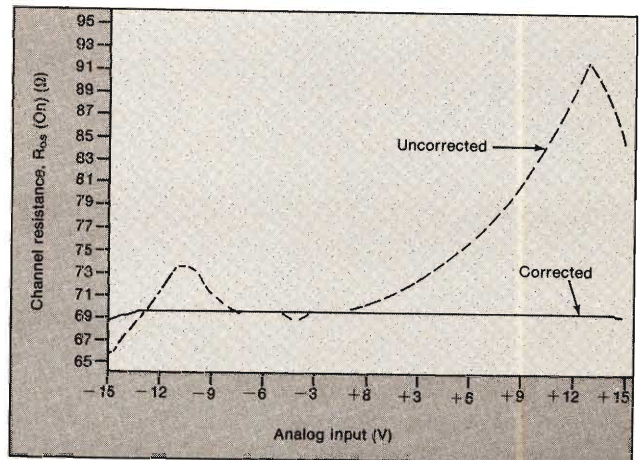
However, high-impedance loads are not always possible or desirable. For example, an rf source must be terminated by 50 or 75 Ω to avoid standing-wave problems on the feed line. Also, audio lines often must be terminated by low-impedance loads to minimize rf and other forms of interference.

The bootstrapped circuit uses a unity-gain operational amplifier, the 741, to provide a signal sample to a floating ground. Because switch resistance is a function of V_{DD} , as well as the signal voltage, the signal can be used to vary the supply voltage to the analog switch, which makes the resistance independent of the signal voltage.

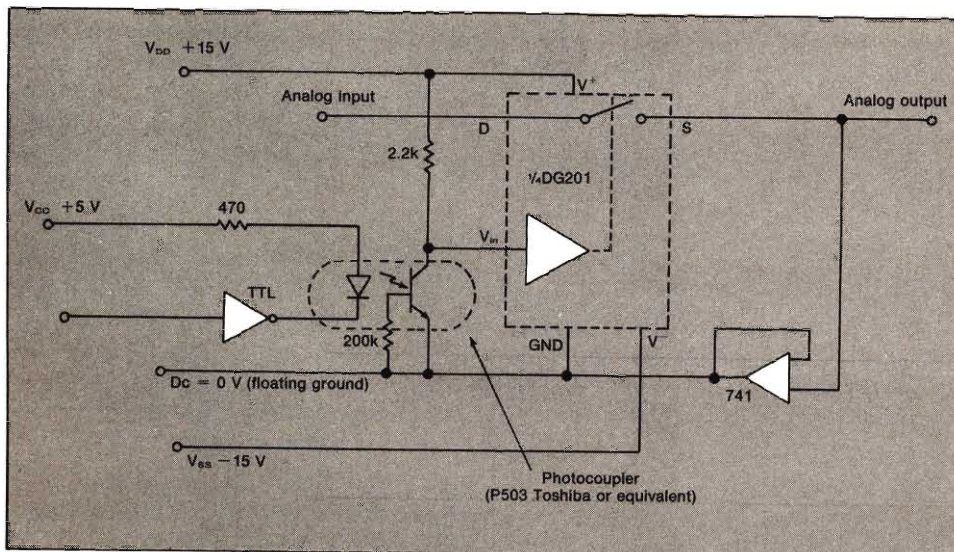
Figure 2 shows the effect of this scheme on channel resistance, $R_{DS(on)}$, over a wide range of input

voltages. The resistance plots contrast the performance of an unmodified analog switch with the bootstrapped version.

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2. Although an uncorrected CMOS analog switch has an on-channel resistance variation of 24 Ω , the corrected version exhibits almost no change.



1. A bootstrapped circuit that provides a constant on-channel resistance minimizes the harmonic distortion common to analog switches terminated by low-impedance loads.

stable condition in the Z80's daisy-chained interrupt priority structure, the circuit has been designed so that an interrupt status signal cannot change when the Machine Cycle 1 line, \overline{M}_1 , is low.)

An active-low interrupt request signal (\overline{INT}) from the support chip is sent to the CPU system through IC₅, an inverter, to indicate the start of the cycle. The interrupt acknowledge line (INTA) from the 8086 or 8088 system is connected to the clock inputs of dual flip-flops IC_{1A} and IC_{1B}, as well as to an OR gate, IC₃. Therefore, when the first INTA pulse ends, \overline{M}_1 goes

low. At the start of the second pulse, the I/O Request line (\overline{IORQ}) also goes low. The requesting device with the highest priority is allowed to place its interrupt vector on the data bus and set an internal latch that indicates the interrupt is under service.

At the end of the second pulse, the Q₂ output from flip-flop IC_{1B} goes low, resetting IC_{1A}, as well as \overline{M}_1 and \overline{IORQ} . A third flip-flop, IC_{2A}, samples the Q₂ output from IC_{1B} and resets the latter device at the end of the cycle. The length of the reset pulse is determined by the frequency of the clock used by IC_{2A}.

TI-59 program finds elliptic transfer function for low-pass filters

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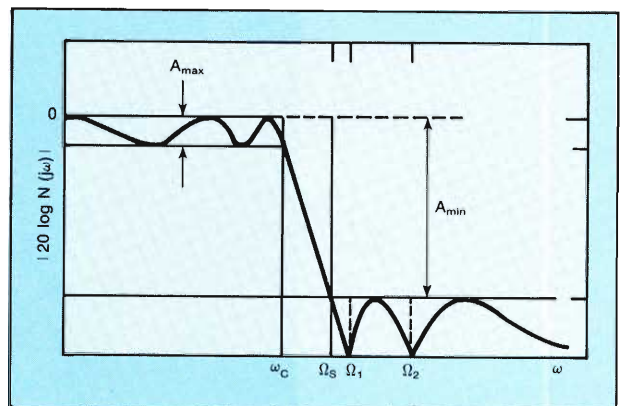
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Of all filtering functions, the elliptic transfer function is among the most useful because of its steep fall-off at the band edges (see the figure). A program designed for the TI-59 calculator can help evaluate the function by finding the odd-order poles and zeros of a low-pass filter (see the program). The algorithm calculates several things:

- The transmission zeros— ΩK , where $K = 1, 2, \dots, (N-1)/2$;
- The minimum attenuation at the stop band with respect to the maximum value at the pass band A_{\min} expressed in dB;

- The real poles (P_0);
 - The complex-conjugate poles (P_K)
- The conjugate poles are equal to $\alpha_K + j\beta_K$, where α_K is the real part and β_K is the imaginary part of the K^{th} pole.

Data supplied by the user (Table 1) includes the order of the filter (that is, the number of poles, or N); the cut-off frequency (ω_c), express-



A calculator program determines the poles and zeros of an elliptic transfer-function filter, one characterized by its steep fall-off at the band edges.

DESIGN SOLUTIONS

ed in radians/s; the stop-band frequency (Ω_s), expressed in radians/s; and either the reflection coefficient (ρ), shown as a percentage, or the maximum attenuation of the pass-band ripple in dB (A_{max}).

The last two of those parameters are related to each other by the formula:

$$A_{max} = -10 \log \left[1 + \left(\frac{\rho}{100} \right)^2 \right]$$

Once the poles and the zeros have been found, the transfer function, $H_{(s)}$, is found with the help of the formula:

$$H_{(s)} = \frac{(S^2 + \Omega_1^2)(S^2 + \Omega_2^2) \dots (S^2 + \Omega_{(N-1)/2}^2)}{(S + P_0)(S + P_1)(S + P_1^*) \dots (S + P_{(N-1)/2})(S + P_{(N-1)/2}^*)}$$

The results obtained with the calculator program for a normalized low-pass filter—that is, one with a ω_c of 1—compare favorably with those found in other filter tables (Table 2). Values other than unity can be used. The program, which can be recorded on a magnetic card, can evaluate the elliptic transfer filtering function up to the 21st order.

*S. Darlington, "Simple Algorithms for Elliptic Filters and Generalizations Thereof," *IEEE Transactions on Circuits and Systems*, Vol. CAS-25, No. 12, pp. 975-980, 1978.

Table 1. User instructions for low-pass elliptic transfer function

Step	Procedure	Enter	Press		Display
1	Filter order	n	A		n
2	Pass-band cut-off frequency (rad/s)	ω_c	B		ω_c
3	Stop-band frequency (rad/s)	Ω_s	C		Ω_s
4a	Either reflection coefficient (%)	ρ	D		0
4b	or passband ripple (dB)	A_{max}	E		0
5	Compute transmission zeros, Ω_k $k = 1, 2, \dots, (n-1)/2$		R/S		Ω_k
	Repeat step 5 for each value of k until 0 appears in the display.				
6	Compute stop-band attenuation, A_{min}		2nd	C'	A_{min}
7	Compute real pole, P_o	0	2nd	D'	P_o
8a	Compute k^{th} pole, real part	k	2nd	D'	Re (P_k)
8b	Compute k^{th} pole, imaginary part		2nd	E'	Im (P_k)
	Repeat steps 8a and 8b for each value of k				
	$k = 1, \dots, (n-1)/2$				

Table 2. Results of calculation for a low-pass filter

Input	Output	
	Zeros	Real and complex poles
n = 5	$\Omega_1 = 1.465436966$	$P_o = -0.3186089933$
$\omega_c = 1$	$\Omega_2 = 1.656220908$	$P_1 = -0.2095320012 + J \quad 0.6875524703$
$\Omega_s = 1.414213562$	$\Omega_3 = 2.165997414$	$P_2 = -0.0582836518 + J \quad 0.991367843$
$\rho = 50\%$	$\Omega_4 = 3.944466518$	
	$A_{min} = 51.4064495 \text{ dB}$	

TI-59 program for filter transfer function

```

000 76 LBL      065 43 RCL      130 95 =      195 04 4      260 95 =
001 11 R      066 08 08      131 39 CDS      196 04 4      261 34 FX
002 42 STD      067 91 R/S      132 55 +      197 42 STD      262 85 +
003 10 10      068 76 LBL      133 43 RCL      198 54 54      263 43 RCL
004 04 4      069 14 D      134 15 15      199 04 4      264 01 01
005 42 STD      070 55 +      135 95 =      200 42 STD      265 35 1/X
006 02 02      071 01 1      136 35 1/X      201 02 02      266 95 =
007 01 1      072 00 0      137 76 LBL      202 02 2      267 65 X
008 02 2      073 00 0      138 34 FX      203 45 YX      268 43 RCL
009 42 STD      074 95 =      139 71 SBR      204 53 (      269 46 46
010 59 59      075 33 X²      140 61 DTD      205 43 RCL      270 95 =
011 43 RCL      076 94 +/-      141 97 DS2      206 10 10      271 71 SBR
012 10 10      077 85 +      142 02 02      207 75 -      272 24 CE
013 91 R/S      078 01 1      143 34 FX      208 01 1      273 65 X
014 76 LBL      079 95 =      144 72 ST*      209 54 )      274 43 RCL
015 12 B      080 28 LOG      145 56 56      210 65 X      275 45 45
016 42 STD      081 65 X      146 35 1/X      211 43 RCL      276 95 =
017 07 07      082 01 1      147 65 X      212 15 15      277 71 SBR
018 91 R/S      083 00 0      148 43 RCL      213 45 YX      278 24 CE
019 76 LBL      084 95 =      149 09 09      214 43 RCL      279 65 X
020 13 C      085 94 +/-      150 95 =      215 10 10      280 43 RCL
021 42 STD      086 76 LBL      151 01 1      216 95 =      281 44 44
022 08 08      087 15 E      152 44 SUM      217 42 STD      282 65 X
023 55 +      088 55 +      153 57 57      218 43 43      283 02 2
024 43 RCL      089 01 1      154 01 1      219 76 LBL      284 95 =
025 07 07      090 00 0      155 44 SUM      220 22 INV      285 55 +
026 95 =      091 95 =      156 56 56      221 71 SBR      286 43 RCL
027 34 FX      092 22 INV      157 43 RCL      222 75 -      287 43 43
028 42 STD      093 28 LOG      158 57 57      223 72 ST*      288 95 =
029 11 11      094 75 -      159 32 X!T      224 54 54      289 35 1/X
030 43 RCL      095 01 1      160 43 RCL      225 32 X!T      290 71 SBR
031 08 08      096 95 =      161 10 10      226 01 1      291 24 CE
032 65 X      097 34 FX      162 22 INV      227 44 SUM      292 45 YX
033 43 RCL      098 42 STD      163 67 EQ      228 54 54      293 43 RCL
034 07 07      099 01 01      164 35 1/X      229 32 X!T      294 10 10
035 95 =      100 00 0      165 00 0      230 97 DS2      295 35 1/X
036 34 FX      101 70 RAD      166 91 R/S      231 02 02      296 95 =
037 42 STD      102 01 1      167 76 LBL      232 22 INV      297 42 STD
038 09 09      103 06 6      168 17 B'      233 43 RCL      298 53 53
039 43 RCL      104 42 STD      169 43 RCL      234 01 01      299 43 RCL
040 11 11      105 56 56      170 10 10      235 33 X²      300 06 06
041 76 LBL      106 00 0      171 42 STD      236 65 X      301 91 R/S
042 85 +      107 42 STD      172 03 03      237 43 RCL      302 76 LBL
043 33 X²      108 57 57      173 01 1      238 47 47      303 19 D'
044 42 STD      109 76 LBL      174 07 7      239 45 YX      304 65 X
045 58 58      110 35 1/X      175 42 STD      240 04 4      305 89 ≠
046 33 X²      111 04 4      176 56 56      241 95 =      306 95 =
047 75 -      112 42 STD      177 76 LBL      242 85 +      307 55 +
048 01 1      113 02 02      178 45 YX      243 01 1      308 43 RCL
049 95 =      114 01 1      179 73 RC*      244 95 =      309 10 10
050 34 FX      115 04 4      180 56 56      245 35 1/X      310 95 =
051 85 +      116 42 STD      181 65 X      246 28 LOG      311 42 STD
052 43 RCL      117 48 48      182 43 RCL      247 65 X      312 02 02
053 58 58      118 43 RCL      183 09 09      248 01 1      313 00 0
054 95 =      119 57 57      184 95 =      249 00 0      314 42 STD
055 72 ST*      120 65 X      185 91 R/S      250 95 =      315 01 01
056 59 59      121 89 ≠      186 02 2      251 94 +/-      316 36 PGM
057 32 X!T      122 95 =      187 44 SUM      252 42 STD      317 05 05
058 01 1      123 55 +      188 56 56      253 06 06      318 17 B'
059 44 SUM      124 53 (      189 97 DS2      254 43 RCL      319 65 X
060 59 59      125 02 2      190 03 03      255 01 01      320 43 RCL
061 32 X!T      126 65 X      191 45 YX      256 33 X²      321 53 53
062 97 DS2      127 43 RCL      192 91 R/S      257 35 1/X      322 95 =
063 02 02      128 10 10      193 76 LBL      258 85 +      323 42 STD
064 85 +      129 54 )      194 18 C'      259 01 1      324 50 50

```

(continued on p. 240)

DESIGN SOLUTIONS

(continued from p. 238)

TI-59 program for filter transfer function

325	32	X:1	353	76	LBL	381	85	+	409	42	STD	437	22	INV
326	65	X	354	10	E*	382	01	1	410	04	04	438	44	SUM
327	43	RCL	355	43	RCL	383	95	=	411	36	PGM	439	52	52
328	53	53	356	51	51	384	34	FX	412	04	04	440	92	RTN
329	95	=	357	65	X	385	85	+	413	10	E*	441	76	LBL
330	42	STD	358	43	RCL	386	43	RCL	414	36	PGM	442	61	GTO
331	51	51	359	11	11	387	05	05	415	04	04	443	42	STD
332	05	5	360	95	=	388	95	=	416	17	B*	444	49	49
333	42	STD	361	91	R/S	389	92	RTN	417	73	RC*	445	35	1/X
334	00	00	362	76	LBL	390	76	LBL	418	52	52	446	85	+
335	01	1	363	75	-	391	54)	419	65	X	447	43	RCL
336	05	5	364	42	STD	392	43	RCL	420	02	2	448	49	49
337	42	STD	365	55	55	393	50	50	421	95	=	449	95	=
338	52	52	366	35	1/X	394	42	STD	422	35	1/X	450	55	+
339	76	LBL	367	85	+	395	01	01	423	42	STD	451	02	2
340	53	(368	43	RCL	396	43	RCL	424	03	03	452	95	=
341	71	SBR	369	55	55	397	51	51	425	00	0	453	55	+
342	54)	370	95	=	398	42	STD	426	42	STD	454	73	RC*
343	97	DS2	371	55	+	399	02	02	427	04	04	455	48	48
344	00	00	372	02	2	400	36	PGM	428	36	PGM	456	95	=
345	53	(373	95	=	401	05	05	429	04	04	457	32	X:1
346	43	RCL	374	34	FX	402	15	E	430	13	C	458	01	1
347	50	50	375	92	RTN	403	43	RCL	431	42	STD	459	22	INV
348	65	X	376	76	LBL	404	50	50	432	50	50	460	44	SUM
349	43	RCL	377	24	CE	405	42	STD	433	32	X:1	461	48	48
350	11	11	378	42	STD	406	03	03	434	42	STD	462	32	X:1
351	95	=	379	05	05	407	43	RCL	435	51	51	463	92	RTN
352	91	R/S	380	33	X ²	408	51	51	436	01	1			

Five-transistor amplifier boosts fast pulses into 50-Ω coaxial cable

M.U. Khan

Manager of Research and Development
Systronics
89-02, Naroda Industrial Area, Naroda-382 330,
Ahmedabad District, India

A simple five-transistor pulse amplifier delivers 5-V pulses into a 50-Ω load, with rise times of just 2.6 ns and fall times of 3.5 ns, matching the performance of more costly circuits containing more parts. Simply by vary-

ing the supply voltage over a range of 6 to 14 V and adjusting the circuit's off-board attenuator, the pulse amplitude can be reduced to as little as 100 mV.

The circuit (see the figure) works from dc to 50 MHz and will deliver pulses as short as 10 ns. It is driven by a TTL signal through a 740S00 quad Schottky NAND gate, IC_A through IC_D. If, however, only an ECL-level signal is available, a level translator, such as the MC10125, can be substituted for the 74S00.

Transistor Q₁, wired as a common-emitter

Obtain accurate ratios with standard resistors

Robert R. Boyd
Hughes Aircraft Co., Ground Systems Group
Fullerton, CA 92634; (714) 732-8058.

When choosing resistor values for voltage dividers, designers usually select a convenient value for one resistor—such as 1 k Ω , 10 k Ω , and so forth—and solve for the other in terms of the required divider ratio. But that procedure typically results in a nonstandard value for the second resistor in the divider. The problem is that custom resistors with nonstandard values are expensive.

Most of the time, though, some combined standard values can supply very close to the desired ratio. With a calculator or computer program, a user can select the resistor pair to a desired degree of accuracy—standard values of 2%, 1%, and 0.1%—and avoid the cost of custom resistors. More universally applicable, though, is a comprehensive list (*see the table*).

Given are values for ratios, D, from 0.01 to 0.49, and users must supply the appropriate decade value. For values of $0.51 \leq D \leq 0.99$, merely enter the table with the value 1-D and reverse the values listed for R_1 and R_2 . (Of course, for $D = 0.5$, $R_1 = R_2$.)

Accordingly, if the ratio $D = 0.9$, from the ratio column on the listing at $D-1 = 0.1$ for a 2% tolerance, select from the $R_1 = 1.87$ and from the R_2 column the value for $R_2 = 16.9$. Of course, these values must be multiplied by the appropriate decade to 1.87 k Ω and 16.9 k Ω , or say, 18.7 k Ω and 169 k Ω , as required, thereby allowing the divider to draw a current level suited to the design. The usual method with standard resistor sizes would have given $R_1 = 1.0$, and $R_2 = 9.09$, the closest standard value, giving a 0.9009 ratio.

The ratios obtained with values from the table are more accurate: 0.9004 from the 2% column, 0.9003 from the 1% column, and 0.9000 (exact) from the 0.1% column.

Standard-resistor ratios						
Ratio (D)	Tolerance					
	2%		1%		0.1%	
	R_1	R_2	R_1	R_2	R_1	R_2
0.01	100.00	1.00	100.00	1.00	198.00	2.00
0.02	56.20	1.15	137.00	2.80	102.00	2.08
0.03	36.50	1.15	280.00	8.66	38.80	1.20
0.04	27.40	1.15	102.00	4.22	24.00	1.00
0.05	24.90	1.33	21.50	1.13	23.40	1.23
0.06	17.80	1.15	21.50	1.37	17.40	1.11
0.07	115.00	8.66	18.20	1.37	18.20	1.37
0.08	11.50	1.00	11.50	1.00	11.50	1.00
0.09	10.00	1.00	10.00	1.00	18.20	1.80
0.10	16.90	1.87	10.20	1.13	9.09	1.01
0.11	13.30	1.62	17.40	2.15	8.98	1.11
0.12	11.50	1.54	11.00	1.50	11.00	1.50
0.13	13.30	1.96	11.30	1.69	10.70	1.60
0.14	11.50	1.87	10.70	1.74	12.90	2.10
0.15	16.20	2.87	11.30	2.00	10.20	1.80
0.16	13.30	2.49	10.50	2.00	10.50	2.00
0.17	18.70	3.83	18.70	3.83	18.70	3.83
0.18	11.50	2.49	13.70	3.01	13.70	3.01
0.19	4.87	1.15	4.32	1.02	19.10	4.48
0.20	16.90	4.22	10.20	2.55	10.20	2.55
0.21	11.50	3.01	4.02	1.07	4.02	1.07
0.22	4.02	1.15	11.50	3.24	11.50	3.24
0.23	3.83	1.15	3.57	1.07	6.26	1.87
0.24	19.60	6.19	4.75	1.50	3.61	1.14
0.25	11.50	3.83	10.20	3.40	3.12	1.04
0.26	11.50	4.02	10.20	3.57	3.70	1.30
0.27	11.50	4.22	3.09	1.15	3.65	1.35
0.28	11.50	4.42	2.74	1.07	3.24	1.26
0.29	11.50	4.64	2.49	1.02	10.70	4.37
0.30	11.50	4.87	2.49	1.07	2.80	1.20
0.31	11.50	5.11	2.55	1.15	3.65	1.64
0.32	11.50	5.36	2.43	1.15	2.21	1.04
0.33	11.50	5.62	2.80	1.37	4.02	1.98
0.34	11.50	5.90	2.67	1.37	1.98	1.02
0.35	11.50	6.19	10.70	5.76	2.34	1.26
0.36	4.64	2.61	4.32	2.43	2.08	1.17
0.37	1.96	1.15	1.96	1.15	1.89	1.11
0.38	1.87	1.15	1.74	1.07	10.10	6.19
0.39	1.78	1.15	2.15	1.37	13.70	8.76
0.40	1.96	1.33	1.50	1.00	1.50	1.00
0.41	11.50	7.87	1.54	1.07	1.54	1.07
0.42	11.50	8.25	1.58	1.15	1.45	1.05
0.43	2.15	1.62	2.15	1.62	1.67	1.26
0.44	1.40	1.10	1.40	1.10	1.40	1.10
0.45	1.62	1.33	1.62	1.33	1.43	1.17
0.46	1.96	1.69	1.33	1.13	1.35	1.15
0.47	1.69	1.47	6.98	6.19	5.30	4.70
0.48	1.15	1.05	1.62	1.50	1.30	1.20
0.49	1.69	1.62	1.69	1.62	2.32	2.23

CIRCLE 521 GET START-AND-RUN VOLTAGES FOR MOTORS

CARL SPEAROW

Sundstrand Corp., 4747 Harrison Ave., Rockford, IL 61125; (815) 394-3263.

Here's a timed two-voltage circuit that can start and run a small dc motor or solenoid. The circuit is simpler than a previously published circuit that performs the same function—it uses one regulator instead of two and fewer other functions (ELECTRONIC DESIGN, April 28, p. 122). The input voltage to the LM317 three-terminal regulator ranges from 5 to 40 V, and the output voltage can range from 2 to 36 V (see the figure).

With an input voltage (V_{in}) initially applied to the input, and the capacitor C_1 in a discharged state, the LM393 comparator's open-collector output circuit is open circuited. Then, the higher start-up output voltage is

$$V_{out1} = 1.25 [1 + (R_3/240)]$$

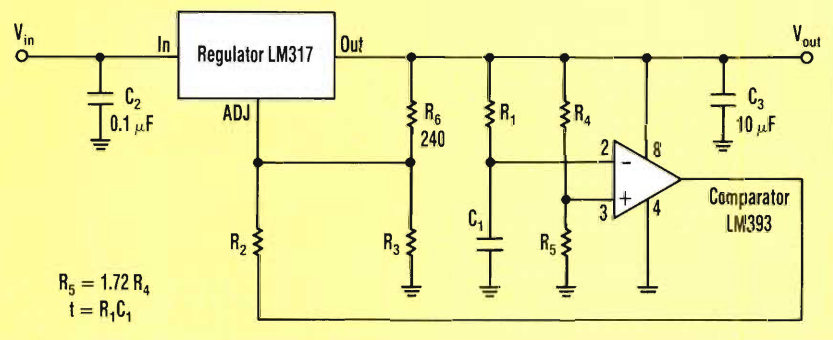
At a time t after start-up, when $t = -R_1 C_1 \ln [R_4 / (R_4 + R_5)]$ or

$t = R_1 C_1$, if $R_5 = 1.72 R_4$ the comparator output goes low. At that time, the output voltage switches to a lower value

$$V_{out2} = 1.25 \{1 + [R_2 R_3 / 240 (R_2 + R_3)]\}$$

for running the device at its proper operating level. □

START AND RUN POWER SOURCE



IN THIS TIMED, two-voltage circuit, the input voltage can range from about 5 to 40 V, and the output voltage can range from about 2 to 36 V at 1.5 A. The circuit is useful for starting dc motors or solenoids. In these applications, one voltage is required to start the device; a different voltage is required to run it.

CIRCLE 522 STANDARD RESISTORS GIVE ACCURATE RATIOS

ROBERT BOYD

Hughes Aircraft Co., 1901 Malvern St., Fullerton, CA 92634; (714) 732-8058.

A simple program written in standard Basic quickly calculates feedback resistors to get accurate gain values for inverting and noninverting op amps and resistors (see the program listing). It also gets accurate ratios for voltage dividers, when using standard resistor values. In fact, a

table of resistor ratios was calculated with this program (ELECTRONIC DESIGN, May 12, p. 154). With no restrictions on the number of decimal places in gain between the limits, the program supplies the most accurate resistor value combinations for the following configurations:

Configuration	Gain (G)	Limits for G (volt/volt)
Voltage divider	$1 / (1 + R_1 / R_2)$	0.01 to 0.99
Inverting op-amp	$-R_2 / R_1$	-100 to -0.01
Noninverting op-amp	$1 + R_2 / R_1$	1 to 100

In operation, the program begins by asking the user for the percent tolerance of the resistors to be

PROGRAM LISTING

```

10 REM Accurate gain ratios - dividers/op-amps
20 F5 = 0:REM Swap R1 & R2 if F5 = 1
30 DEF FNA(X) = .01*INT(X*100+.5)
40 DEF FNB(X) = .1*INT(X*10+.5)
50 DEF FNC(X) = INT(X+.5)
60 REM Roundoff routines
70 INPUT "2, 1, or 0.5% ";B
80 INPUT "Gain ? ";G
90 IF G = -1 THEN R1 = 1:R2 = 1:GOTO 350
100 IF G = 1 THEN R1 = 1:R2 = 0:GOTO 350
110 IF G < 0 THEN A = -1/G:GOTO 150
120 IF G < 1 THEN A = 1/G-1:GOTO 150
130 IF G < 2 THEN A = 1/(G-1):GOTO 150
140 A = G-1:F5 = 1
150 B = 96/B
160 REM B = No. of discrete resistor values, 48, 96 or 192
170 E = B
180 REM Initialize error E
190 IF A < 1 THEN A = 1/A:F5 = 1
200 L = FNC(B*LOG10(A))
210 FOR M = 1 TO B
220 N = L + M - 1
230 R8 = 10^(N/B)
240 REM R8 = trial value of R1
250 IF N < = B THEN R8 = FNA(R8)
260 IF N > B AND N < = 2*B THEN R8 = FNB(R8)
270 IF N > 2*B THEN R8 = FNC(R8)
280 REM Insures just 3 significant figures
290 R9 = FNA(10^((M-1)/B)):E1 = ABS(R8/R9-A)
300 REM R9 = trial value of R2
310 IF E1 < E THEN E = E1:R1 = R8:R2 = R9
320 REM Find smallest error E
330 NEXT M
340 IF F5 = 1 THEN S = R1:R1 = R2:R2 = S
350 PRINT G; R1;R2
360 END
    
```

VOTE!

Read all the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a \$150 Best-of-Issue award and becomes eligible for a \$1,500 Idea-of-the-Year award.

used—2%, 1%, or 0.5%—with the 0.5% tolerance supplying the same accuracy as 0.1% resistors would. Next, the program asks for the gain G in volt/volt. The requested gain determines the program branching to one of the three circuit configurations:

Gain	Branches to
$G < 0$	Inverting op-amp
$0 < G < 1$	Voltage divider
$G > 1$	Non-inverting op-amp

After the user enters the percentage values and gain, the program operates for a time interval inversely proportional to the resistor tolerance: The smaller the tolerance, the longer it takes. The resulting resistor values supply standard resistor values and tolerances.

The Basic program takes the following approach: It establishes two resistor variables— $R_x = 10^{(n-1)/B}$ and $R_y = 10^{(m-1)/B}$ —where $n > m > 1$ and $B = 48$ for 2%, 96 for 1%, and 192 for 0.5% tolerance. Then, where $A = R_x/R_y$, $B \cdot \text{Log } A = n - m$. Because the standard resistor values require that

n and m must be integers, the result difference— $\text{INT}(n-m) = N - M$ —only approximately equals $B \cdot \text{Log } A$.

Accordingly, the program calculates discrete trial values of R_1 and R_2 for integer M and N values during iterations of M from 1 to B . Using these trial values of R_1 and R_2 , the program makes a comparison of their ratio R_1/R_2 with the ideal continuous ratio A . The program saves the trial values of R_1/R_2 that minimize the error $(R_1/R_2) - A$ and prints them out with the requested gain G .

An example run of each of the three configurations with 1% resistors delivers zero-error results.

Configuration	G	R_1	R_2
Voltage divider	0.24	4.75	1.50
Inverting op amp	-0.68	1.50	1.02
Noninverting op amp	1.70	1.50	1.05

Of course, the user must supply the appropriate decade value for each resistor, such as 475 Ω , 4.75k, or 475k, in the actual circuit. □

for every pulse received.

The Q output signals from IC4 turn on AND gate IC7d to pass bursts of crystal-controlled 100-Hz signals from the MM5369EST oscillator chip IC5. The output of IC7d feeds to a 12-stage binary counter IC9, a CD4040. Since the maximum period of the low-frequency signal is 6 s, the circuit must use 10 bits of the counter to count to 600 (2^{10} equals

PROGRAM FOR THE EPROM

Hexa-decimal Address	Hexa-decimal Data	Hexa-decimal Address	Hexa-decimal Data
4B	80	80	47
4C	79	81	47
4D	78	82	46
4E	77	83	46
4F	76	84	46
50	75	85	45
51	74	86	45
52	73	87	45
53	72	88	44
54	72	88	44
55	71	8A	44
56	70	8B	44
57	69	8C	43
58	68	8D	43
59	68	8E	43
5A	67	8F	42
5B	66	90	42
5C	65	91	42
5D	65	92	41
5E	64	93	41
5F	63	94	41
60	63	95	41
61	62	96	40
62	61	97-9A	39
63	61	9B-9E	38
64	60	9F-A2	37
65	60	A3-A7	36
66	59	A8-AB	35
67	58	AC-B0	34
68	58	B1-B5	33
69	57	B6-BB	32
6A	57	BC-C1	31
6B	56	C2-C7	30
6C	56	C8-CE	29
6D	55	CF-D6	28
6E	55	D7-DA	27
6F	54	DB-DC	06
70	54	DD-F0	25
71	53	F1-FA	24
72	53	FB-104	23
73	52	105-110	22
74	52	111-11D	21
75	52	11E-12C	20
76	51	12D-13B	19
77	51	13C-14D	18
78	50	14E-160	17
79	50	161-177	16
7A	49	178-190	15
7B	49	191-1AC	14
7C	49	1AD-1CD	13
7D	48	1CF-1F4	12
7E	48	1F5-221	11
7F	48	222-258	10

CIRCLE 523 MEASURE BREATHING RATE WITH SENSOR

RICARDO JIMENEZ-GARCIA

Mexicali Technological Institute, 233 Paulin Ave., Box 7953,
Calexico, CA 92231; (619) 357-0974.

To a seriously injured patient or one undergoing surgery, respiratory rate is critical to immediate survival. With a \$12 respiratory sensor placed under an oxygen mask, medical workers can monitor respirations per minute on a liquid crystal display. An audible tone warns of respiratory failure (see the figure).

The sensor is a circuit that detects air pressure. Because the pressure of expired air is higher than that of inhaled air, the sensor, placed in the airway at the bottom of an oxygen mask, can monitor the patient's respiratory flow. The circuit then converts these air-pressure signals to respirations-per-minute readings.

Edmund Scientific sells the device,

an ultrasensitive 0.004-psi air-pressure switch (Catalog No. E36,839). Single-pole, normally open switch contacts on the sensor are rated to handle 20 mA. The sensor's input port accepts 1/8-in. inside-diameter tubing (Catalog No. E35,918), which connects to the airway in the oxygen mask.

A 7555 timer IC1, configured as a monostable multivibrator, gives a 0.1-s positive, square output pulse each time a monitored person exhales and the sensor switch closes. This positive pulse enables timer IC2, a 5-kHz oscillator that drives a piezoelectric buzzer, to produce an audible tone for every pulse received. The positive pulse also triggers flip-flop IC4 to change its state

load. An FET source follower can isolate the Iso-Gate output from the large input capacitance of the MOSFET to improve the circuit's speed. Or if the application doesn't need the full 50-W load capability, the circuit can use a smaller die-sized MOSFET.

Also, the AD204 has isolated ± 7.5 -V power available on the load side for other circuitry. For instance, that power could supply an LP311 comparator on the load side to make an undervoltage-lockout or overcurrent-limit circuit. □

amount back to pin 5 reduces the gain. Even with the added op amp in the feedback path, the stability of the circuit is excellent (Fig 2).

To better understand the circuit's operation, consider the INA117 to be a four-input device where E_2 is the signal at pin 2; E_3 at pin 3; E_5 at pin 5; and so forth. The output voltage is: $E_0 = E_3 - E_2 + 19E_5 - 18E_1$.

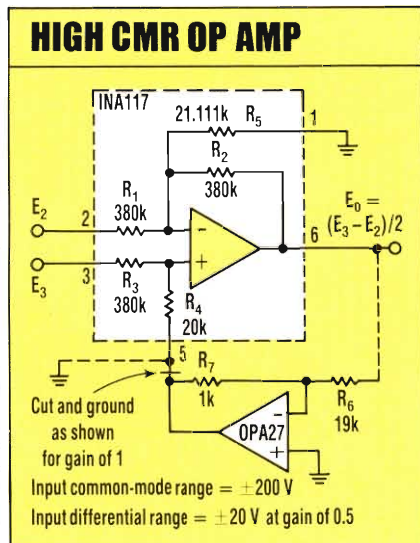
With E_1 grounded (equal to 0 V) the reduced differential gain is: $A = 1/[1+19/(R_6/R_7)]$ and for $A = 0.5$, $R_6/R_7 = 19$.

Because of the low output impedance of the OPA27 circuit, the impedance at pin 5 of the INA117 is low. Consequently, the INA117's critical resistor matching, gain, and common-mode rejection are preserved. To adjust the common-mode rejection for critical applications, add a 10- Ω fixed resistor in series with pin 5 and a 20- Ω variable resistor in series with pin 1. Short pins 2 and 3 together and drive them with a 500-Hz square wave. A square wave instead of a sine wave allows the ac signal to settle out and makes the dc CMR easier to observe on an oscilloscope and adjust. At high gain, trim the circuit to minimum output with the 20- Ω variable resistor. This trimming of the CMR may change the gain slightly. If it does, then adjust the R_6/R_7 ratio to adjust gain. This adjustment will not affect the CMR. □

CIRCLE 526 OP AMP HANDLES HIGH COMMON-MODE VOLTS

R. MARK STITT

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85710; (602) 746-7412.



1. THIS MONOLITHIC

difference amplifier can accept common-mode input signals as high as ± 200 V, though it operates from standard ± 15 -V power supplies.

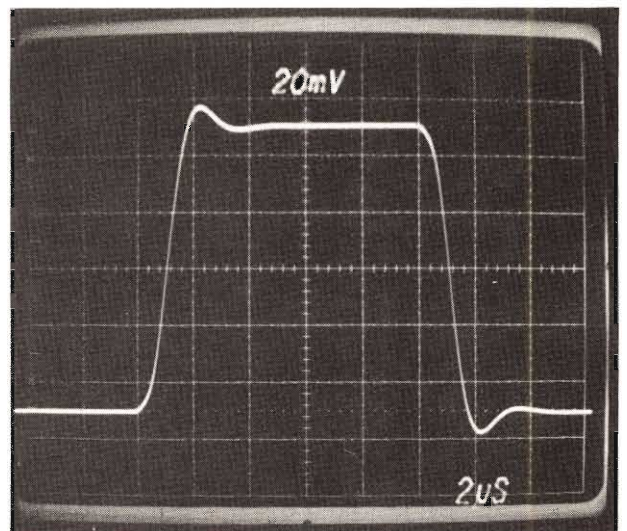
The INA117, a monolithic difference amplifier, can accept common-mode input signals to ± 200 V, though it operates from standard ± 15 -V power supplies. Many applications require an amplifier with both a high common-mode and a differential-input capability.

This high common-mode-rejection capability results from the roughly 20-to-1 resistor dividers internally supplied on the inputs of the op amp (Fig. 1). With that attenuation, a ± 200 -V common-mode signal reduces to ± 10 V at the op amp's two inputs. This arrangement rejects the common-mode signal, but passes dif-

ferential signals at unity gain. The proper resistors in the op-amp circuit can set the gain independently of the common-mode-rejection ability. But for the gain to remain stable with temperature changes, the ratios of R_1/R_2 and R_3/R_4 must track with ratio $R_1/(R_2$ in parallel with $R_5)$.

The circuit, however, limits the INA117's differential input range to about ± 12 V, only because it has unity gain. Its ± 15 -V power supplies limit the output swing. Reducing the gain would increase the differential input range. For example, if the gain were reduced to 0.5, that would increase the circuit's differential input range to ± 20 V.

Reducing the gain just with external resistors may seem like a simple approach, but the external op-amp (OPA27) circuit for reducing the gain is much better. It preserves the INA117's extremely precise internal-resistor matching, so the circuit's common-mode rejection and its drift with temperature remain unchanged. Furthermore, the gain-reduction produced by the external op-amp circuit improves output noise. It would remain unchanged with the simpler approach. Inverting the output with the OPA27 and feeding a small



2. EVEN WITH THE OPA27 OP-AMP

feedback circuit gain of 0.5, and 1000-pF load, the stability of the INA117 circuit is excellent.

IdeasForDesign

Compensator cancels cold-junction errors

A thermocouple cold-junction compensation circuit consisting of an LM10B dual voltage reference and operational amplifier and an AD590J temperature-sensitive current source proves useful when an ice bath is not available by canceling the error that results from having the reference junction at 25°C. It also provides gain to scale the output signal to an approximate ± 5 -V range.

To correct for the reference junction error at 25°C, an offset term and a dv/dt term must be applied. The AD590J, placed in close thermal contact with the reference junction, produces a current that is proportional to absolute temperature. This current corrects for the reference-junction error by flowing through R_1 to produce a correction at the output.

The reference junction also has an offset term that is, in part, corrected by the AD590J's 25°C steady-state current of 298 μ A. The remainder of the current is bled off by the sink composed of a reference amplifier, IC₂, which is connected to provide a constant current.

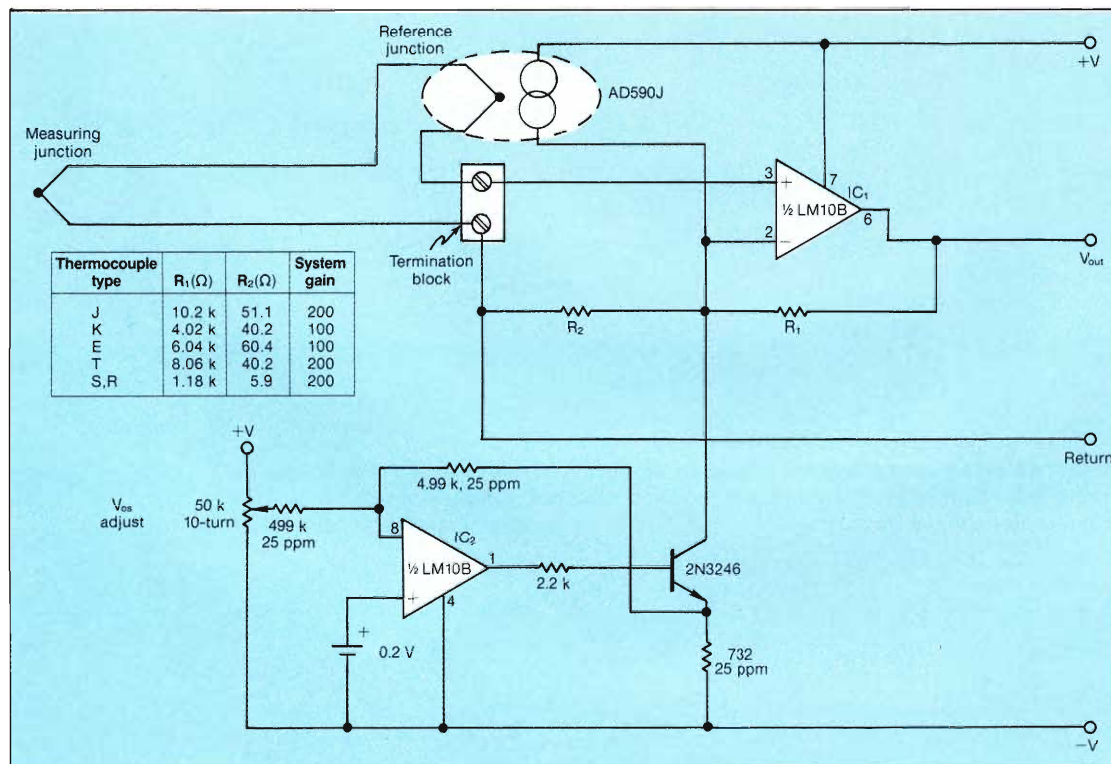
Gain error is a function of the ratio match of

resistors R_1 and R_2 . The absolute value of R_1 determines the accuracy of the cold-junction correction over the expected ambient temperature range. For an ambient range of 25°C, $\pm 10^\circ$ C, a 1% absolute value for R_1 is usually sufficient for a total system error to within $\pm 0.5^\circ$ C over a 15 to 35°C ambient temperature range. The circuit is calibrated by adjusting the 50-k Ω precision trimpot for proper output voltage according to the junction temperature and the circuit gain.

Values for resistors R_1 and R_2 , corresponding to the most popular thermocouple types, are listed in the insert. For other thermocouple types, the value of R_2 can be found from the values of R_1 and the desired gain.

Supply-voltage level for the circuit can range from 5 to 39 V for the positive supply and from -2 to -35 V for the negative supply. However, the spread from +V to -V must not exceed 40 V, the breakdown limit of the LM10B.

Steve Hageman, Project Engineer, E-H International, Inc., 7303 Edgewater Dr., Oakland, CA 94621.



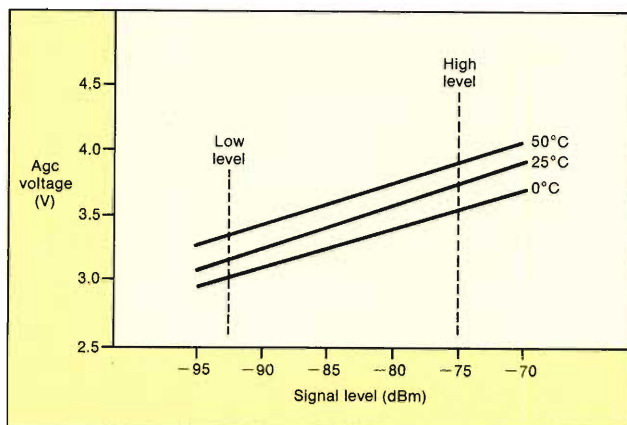
A temperature-sensitive current source, the AD590J from Analog Devices Inc., produces a current that is proportional to absolute temperature and corrects for reference-junction error in this thermocouple cold-junction compensator.

IdeasForDesign

usually at room temperature (25°C). Here the temperature-varying component is zeroed out of the reference voltage by using the zero calibration adjustment potentiometer to set the test-point voltage to zero. The Ref₁ and Ref₂ adjustment must also be set for the desired trip levels. Final calibration is done at either temperature extreme. For example, at the 50°C point the shifting voltage will be at a maximum positive value.

At this point, the gain potentiometer is adjusted to move both trip points back to the desired level. Once calibrated, the temperature-varying characteristic will closely track the changes in the agc voltage curve. For test purposes, the values shown yield a temperature-varying voltage of about 2 to 11 mV/°C as measured at the test point. That range can be modified if desired.

Dean S. Carpenter, Member of Technical Staff, Rockwell International, Collins Communications Systems Division, 3200 E. Renner Rd., CS.7, Richardson, Texas 75081.



2. The agc voltage level varies significantly when temperature changes and the signal level remains constant. Sometimes that difference can be a large part of the assumed voltage change that results from an increase in received signal strength.

Switched-mode amplifier allows isolated dc current measurements

A switching amplifier that reduces the effects of core saturation greatly simplifies the design of a circuit for isolated measurement of dc currents. A ferrite current-sensing transformer ensures the isolation, and a slightly modified single-chip astable multivibrator helps deliver a voltage output that is proportional to the dc current passing through the transformer. The polarity of the voltage changes when the current changes direction.

The circuit, which also measures low-frequency ac currents, is suitable in any type of power-converting equipment. For example, it measures current in dc motor drives with silicon controlled rectifiers, as well as in servo motors with pulse-width modulation (PWM) converters. Another typical application is a variable-frequency induction motor drive.

Other techniques for providing isolated dc current measurement also rely on a current-sensing transformer, but they usually need two cores: one through which the dc current flows and another that forces the H-field in the first core to be close to zero. In this technique, the core will not be symmetrically magnetized and rather large nonlinearities result.

Two methods overcome that inherent nonlinearity.

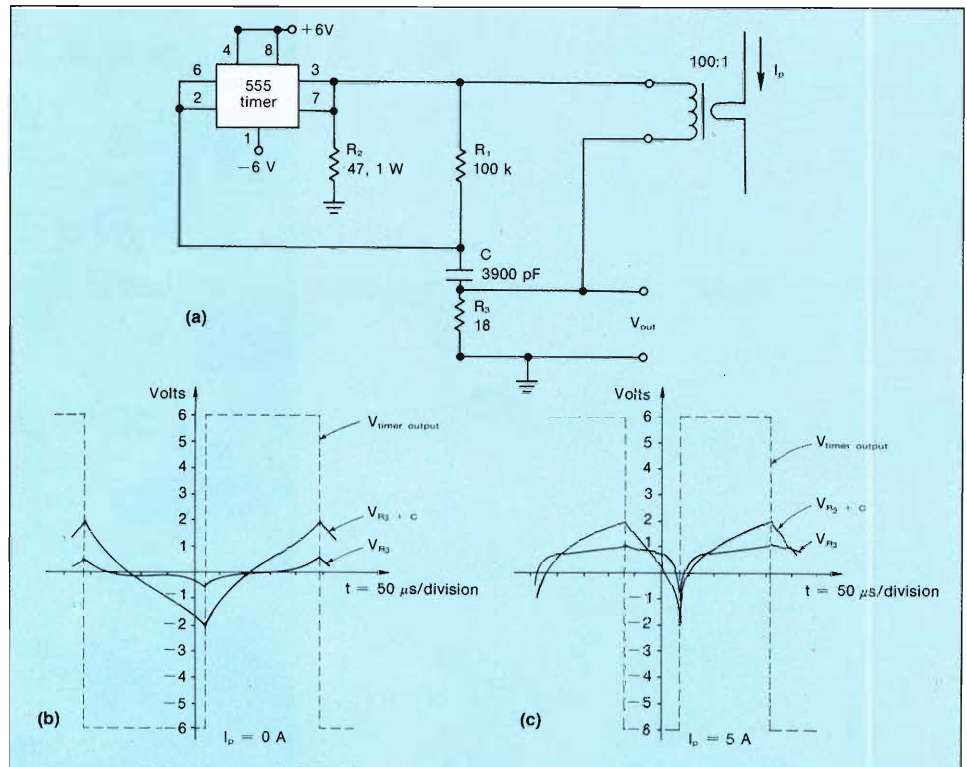
One measures the B-field with a Hall-effect device. The other, shown in Fig. 1, uses a single core. The key to linear dc current measurement is a switching amplifier—a 555 timer—that symmetrically saturates the core. Thus the mean value of the magnetizing current is zero, and that of the secondary current is theoretically equal to the primary current times the turns ratio of the transformer. The current-sensing transformer thus becomes very insensitive to offsets and nonlinearities and to temperature-dependent core characteristics.

The circuit, an astable multivibrator, uses the timer with two additional resistors, R₂ and R₃. A Pulse Engineering PE 51687 or a Supermalloy Magnetics 52011-1/2 F toroidal transformer will produce good results, but any pulse transformer that acts as a current transformer can be used.

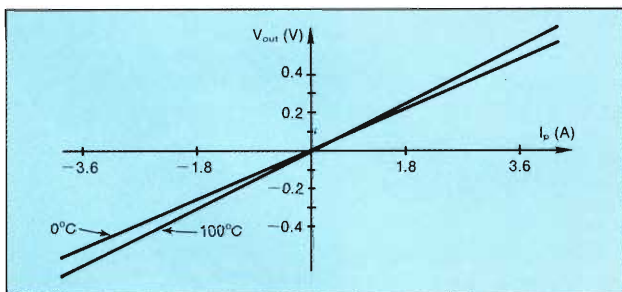
Resistor R₂ provides a positive output current from the timer when the chip's output voltage is high. The reverse is also true. If the dc current is unidirectional, a diode can be inserted in series with R₂ to reduce power losses and increase the current in the secondary winding.

The feedback voltage to pins 2 and 6 is the sum

IdeasForDesign



1. By negating the nonlinear effects of core saturation in a current-sensing transformer, a simple astable multivibrator circuit permits the transformer to be used in making reliable, isolated measurements of dc or ac currents. Correct adjustment of the multivibrator's frequency ensures that the transformer core is slightly saturated before each switching of the timer IC's output (traces a and b).



2. Nonlinearity of the output voltage readings is not great, despite the extreme temperature differences of the transformer core. Some toroidal cores will be even less sensitive to temperature variations.

of the voltages across C and R_3 . The oscillator frequency, determined by the time constant of R_1 and C, should be set significantly lower when the transformer is disconnected—about 20% to 50% less than when the transformer is wired into the circuit. In this way, the core is slightly saturated before each switching of the timer's output, as shown in the oscilloscope-trace diagrams of Fig. 1.

Figure 2 illustrates the changes that can be expected in measurements as a result of temperature variation in the ferrite core. The range shown is

rather extreme, yet variations are not excessive. When the transformer is connected, the oscillator frequency is 1.9 kHz at 0°C and 3.2 kHz at 100°C. Small tape-wound, square toroidal cores, such as the Supermalloy, give an almost-zero temperature sensitivity and reduce the need for filtering of the output voltage, V_{out} .

Tore M. Undeland, Norwegian Institute of Technology, Department of Electrical Engineering, Power Electronics Section, N-7034 Trondheim—NTH, Norway.

Reference:

1. Anders Gytri and Tore M. Undeland, "Low-Cost DC and AC Current Transducer with Isolation and Good Linearity," *PCI Proceedings*, March 1982, pp. 341–353.

Winner for August 5, 1982

"One-chip slope-delta modem is good for low-frequency jobs"

Dan Baker, Principal Engineer, Litton Microwave Cooking Products, 1405 Xenium Lane N., Minneapolis, Minn. 55441.

IdeasForDesign

The optional momentary clear switch, S_5 , causes all F's with decimal points to be clocked into the display. This feature is useful, since any received character, including an F, will extinguish the decimal point.

Expansion of the circuit to more than six characters is straightforward. The additional benefits, however, must be weighed against the increased cost

of the parts and the current drain of additional LED readouts.

Michael J. Kavaya, Senior Scientist, Jet Propulsion Laboratory, California Institute of Technology, 4800 Oak Grove Dr., Pasadena, Calif. 91109. Hardy C. Martel, Professor of Electrical Engineering, and William C. Snyder, California Institute of Technology, 116-81, Pasadena, Calif. 91125.

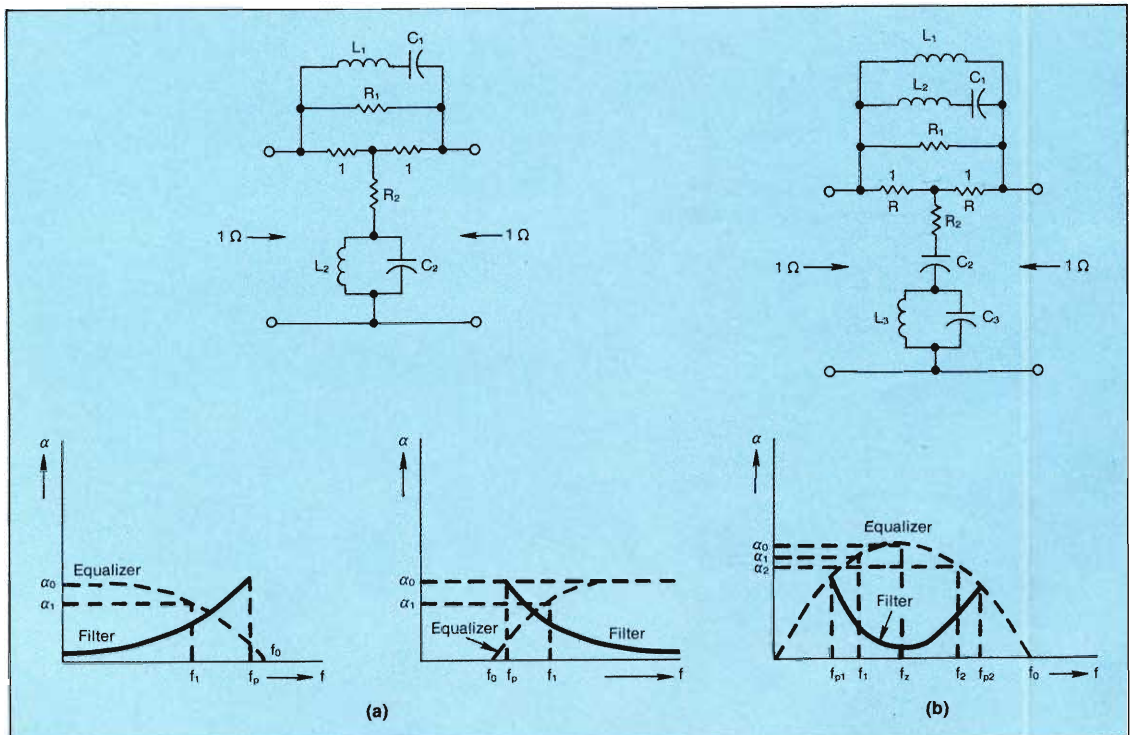
Program in Basic speeds design of equalizing networks

A simple program in Basic aids the quick design of equalizing networks for low-pass, high-pass, and bandpass filters. Such equalizers ensure a flat system response in the passband of interest and meet the requirements of modern telecommunications systems.

Normalized component values for the most popular equalizer, the bridged-T, are found with the help of the networks in Fig. 1. A suitable equalizer for a high- or low-pass filter circuit is shown in Fig.

1a, while the design of an equalizer for a bandpass filter is represented in Fig. 1b.

Given the basic attenuation of the equalizer used with a high-pass or low-pass filter, α_0 , the pole position (f_0) of its admittance function, y , and the equalizer's attenuation, α_1 , at the selected reference frequency (f_1), the program will find the value of resistor R_1 from the relation $\alpha_0 = 1n(1+r_1)$. The value of capacitor C_1 , can be found from both

$$y(s) = C_1s/(L_1C_1s^2+1)$$


1. The system response of a filter can often be improved with a bridged-T network equalizer. Configurations for low-pass and high-pass filters (a) and bandpass filters (b) are possible. A program in Basic will determine the component values from the equalizer's maximum attenuation, its frequency of minimum attenuation from the pole position, and from the desired attenuation at one or two selected frequencies.

IdeasForDesign

Basic program for designing an equalizer

```
LISTNH
10 REM-DESIGN OF ATTENUATION EQUALIZER FOR FILTERS
20 DIM W(20)
30 PRINT "JOB:";
40 INPUT .0#
50 PRINT "-----"
60 PRINT "TERMINATING IMPEDANCE(OHMS) =";
70 INPUT R
80 PRINT "TYPE OF FILTER- LOW PASS & HIGH PASS (1), BAND PASS (2);";
90 INPUT T
100 PRINT
110 PRINT "BASIC ATTENUATION (DBS) =";
120 INPUT A0
130 F=EXP(A0/8.686)
140 R1=R*(F-1)
150 R2=R/(F-1)
160 F INT "POLE POSITION (MHZ) =";
170 INPUT W0
180 IF T=2 THEN 330
190 PRINT "REFERENCE FREQ.(MHZ) AND ATTENUATION (DBS) =";
200 INPUT W1,A1
210 B=EXP(A1/4.343)
220 Y=SQRT((B-F^2)/((F-1)^2*(1-B)))
230 X=ABS(4.28318*W*(W0^2-W1^2)/W1)
240 L1=R/X
250 C1=1/(6.28318*W0)^2*L1)
260 L2=L1/R^2
270 C2=C1*R^2
280 PRINT TAB(5);"R1=";R1;TAB(30);"R2=";R2
290 PRINT TAB(5);"L1=";L1;TAB(30);"C1=";C1
300 PRINT TAB(5);"L2=";L2;TAB(30);"C2=";C2
310 PRINT TAB(5);"TUNING FREQ.(MHZ) OF L1C1 & L2C2 =";W0
320 GO TO 550
330 PRINT "LOWER REFERENCE FREQ.(MHZ) & ATTENUATION(DBS) =";
340 INPUT W1,A1
350 PRINT "UPPER REFERENCE FREQ.(MHZ) & ATTENUATION(DBS) =";
360 INPUT W2,A2
370 B=EXP(A1/4.343)
380 C=EXP(A2/4.343)
390 Y1=SQRT((B-F^2)/((F-1)^2*(1-B)))
400 Y2=SQRT((C-F^2)/((F-1)^2*(1-C)))
410 X1=4.28318*W1*W2*(Y1*W2*(W1^2-W0^2)-Y2*W1*(W2^2-W0^2))/(W0^2*(W1^2-W2^2))
420 X2=6.28318*(Y2*W2-Y1*W1)*(W2^2-W0^2)*(W1^2-W0^2)/(W0^2*(W1^2-W2^2))
430 L1=R/X1
440 L2=R/X2
450 C1=1/(6.28318*W0)^2*L1)
460 C2=L1/R^2
470 L3=C1/R^2
480 C3=L2/R^2
490 Y=60*SQRT(C1/(X1+X2))
500 PRINT TAB(5);"R1=";R1;TAB(30);"R2=";R2
510 PRINT TAB(5);"L1=";L1;TAB(30);"L2=";L2;TAB(55);"C1=";C1
520 PRINT TAB(5);"C2=";C2;TAB(30);"L3=";L3;TAB(55);"C3=";C3
530 PRINT TAB(5);"TUNING FREQ.(MHZ) OF L2C1 & L3C3 =";W0
540 PRINT TAB(5);"TUNING FREQ.(MHZ) OF L1L2C1 & C2L3C3 =";Z
550 PRINT "ALL RESISTORS ARE IN OHMS,"
560 PRINT "CAPACITORS ARE IN MICROFARADS AND INDUCTORS ARE IN MICROHENRIES"
570 PRINT
580 PRINT "ANALYSIS OF THE DESIGN OBTAINED :";
590 PRINT "-----"
600 PRINT "NO. OF FREQUENCIES FOR ANALYSIS =";
610 INPUT N
620 FOR I=1 TO N
630 PRINT "FREQ.(MHZ) =";
640 INPUT W(I)
650 NEXT I
660 PRINT
670 PRINT TAB(5);"FREQ.(MHZ)";TAB(30);"ATTENUATION(DBS)"
680 FOR I=1 TO N
690 IF T=2 THEN 720
700 Y=X*W(I)/(6.28318*(W0^2-W(I)^2))
710 GO TO 730
720 Y=X1/(6.28318*W(I))+X2*W(I)/(6.28318*(W(I)^2-W0^2))
730 A=4.343*LOG(((F/(F-1))^2+Y^2)/((1/(F-1))^2+Y^2))
740 PRINT TAB(5);W(I);TAB(30);A
750 NEXT I
760 PRINT
770 PRINT "IF REDESIGNING IS DESIRED FEED 1 OTHERWISE FEED 0 :";
780 INPUT M
790 IF M=1 THEN 100
800 END
```

IdeasForDesign

Equalizing networks

The following listings are reprints of the programs that appeared as part of a recent Idea for Design entitled "Program in Basic speeds design of equalizing networks" (Sept. 16, p. 178). Because of the great interest in the programs and the difficulty encoun-

tered in printing the original listings, we have reproduced them below in a more readable form. The circuit idea was submitted by A.K. Goyal and C. Rao Kasarbada, both of Indian Telephone Industries Ltd., Uttar, Pradesh, India.

Basic program for designing an equalizer

```
LISTNH
10 REM-DESIGN OF ATTENUATION EQUALIZER FOR FILTERS
20 DIM W(20)
30 PRINT "JOB:";
40 INPUT J$
50 PRINT "-----"
60 PRINT "TERMINATING IMPEDANCE (OHMS) =";
70 INPUT R
80 PRINT "TYPE OF FILTER—LOW PASS & HIGH PASS (1), BAND PASS (2):";
90 INPUT T
100 PRINT
110 PRINT "BASIC ATTENUATION (DBS) =";
120 INPUT AO
130 F=EXP(AO/8.686)
140 R1=R*(F-1)
150 R2=R/(F-1)
160 PRINT "POLE POSITION (MHZ) =";
170 INPUT W0
180 IF T=2 THEN 330
190 PRINT "REFERENCE FREQ. (MHZ) AND ATTENUATION (DBS) =";
200 INPUT W1,A1
210 B=EXP(A1/4.343)
220 Y=SQR((B-F^2)/(((F-1)^2)*(1-B)))
230 X=ABS(6.28318*Y*(W0^2-W1^2)/W1)
240 L1=R/X
250 C1=1/((6.28318*W0)^2*L1)
260 C2=L1/R^2
270 L2=C1*R^2
280 PRINT TAB(5);"R1=";R1;TAB(30);"R2=";R2
290 PRINT TAB(5);"L1=";L1;TAB(30);"C1=";C1
300 PRINT TAB(5);"L2=";L2;TAB(30);"C2=";C2
310 PRINT TAB(5);"TUNING FREQ. (MHZ) OF L1C1 & L2C2 =";W0
320 GO TO 550
330 PRINT "LOWER REFERENCE FREQ. (MHZ) & ATTENUATION(DBS) =";
340 INPUT W1,A1
350 PRINT "UPPER REFERENCE FREQ. (MHZ) & ATTENUATION(DBS) =";
360 INPUT W2,A2
370 B=EXP(A1/4.343)
380 C=EXP(A2/4.343)
390 Y1=SQR((B-F^2)/(((F-1)^2)*(1-B)))
400 Y2=SQR((C-F^2)/(((F-1)^2)*(1-C)))
410 X1=6.28318*W1*W2*(Y1*W2*(W1^2-W0^2)-Y2*W1*(W2^2-W0^2))/(W0^2*(W1^2-W2^2))
420 X2=6.28318*(Y2*W2-Y1*W1)*(W2^2-W0^2)*(W1^2-W0^2)/(W0^2*(W1^2-W2^2))
430 L1=R/X1
440 L2=R/X2
450 C1=1/((6.28318*W0)^2*L2)
460 C2=L1/R^2
470 L3=C1*R^2
480 C3=L2/R^2
490 Z=W0*SQR(X1/(X1+X2))
500 PRINT TAB(5);"R1=";R1;TAB(30);"R2=";R2
510 PRINT TAB(5);"L1=";L1;TAB(30);"L2=";L2;TAB(55);"C1=";C1
520 PRINT TAB(5);"C2=";C2;TAB(30);"L3=";L3;TAB(55);"C3=";C3
530 PRINT TAB(5);"TUNING FREQ. (MHZ) OF L2C1 & L3C3 =";W0
540 PRINT TAB(5);"TUNING FREQ. (MHZ) OF L1L2C1 & C2L3C3 =";Z
550 PRINT "ALL RESISTORS ARE IN OHMS."
560 PRINT "CAPACITORS ARE IN MICROFARADS AND INDUCTORS ARE IN MICROHENRIES"
570 PRINT
580 PRINT "ANALYSIS OF THE DESIGN OBTAINED."
590 PRINT "-----"
600 PRINT "NO. OF FREQUENCIES FOR ANALYSIS =";
610 INPUT N
620 FOR I=1 TO N
630 PRINT "FREQ.(MHZ) =";
640 INPUT W(I)
650 NEXT I
660 PRINT
670 PRINT TAB(5);"FREQ. (MHZ)";TAB(30);"ATTENUATION(DBS)"
680 FOR I=1 TO N
690 IF T=2 THEN 720
700 Y=X*W(I)/(6.28318*(W0^2-W(I)^2))
710 GO TO 730
720 Y=X1/(6.28318*W(I))+X2*W(I)/(6.28318*(W(I)^2-W0^2))
730 A=4.343*LOG(((F-1)^2+Y^2)/((F-1)^2+Y^2))
740 PRINT TAB(5);W(I);TAB(30);A
750 NEXT I
760 PRINT
770 PRINT "IF REDESIGNING IS DESIRED FEED 1 OTHERWISE FEED 0.:";
780 INPUT M
790 IF M=1 THEN 100
800 END
```

Program for an equalizer for a 108-kHz low-pass filter

```
RUNNH
JOB:? SAMPLE RUN (EQUALIZER FOR A 108 KHZ LOW PASS FILTER)
```

```
TERMINATING IMPEDANCE(OHMS) =?150
TYPE OF FILTER— LOW PASS & HIGH PASS (1), BAND PASS (2):?1
```

```
BASIC ATTENUATION (DBS) =?1.8
POLE POSITION (MHZ) =? 1082
REFERENCE FREQ. (MHZ) AND ATTENUATION (DBS) =? 1065.8
R1= 34.5398297202 R2= 651.421856513
L1= 1292.95179486 C1= 1.67341686678E-03
L2= 37.6518795027 C2= .057464524216
TUNING FREQ. (MHZ) OF L1C1 & L2C2 = .1082
```

```
ALL RESISTORS ARE IN OHMS.
CAPACITORS ARE IN MICROFARADS AND INDUCTORS ARE IN MICROHENRIES
```

```
ANALYSIS OF THE DESIGN OBTAINED :
```

```
NO. OF FREQUENCIES FOR ANALYSIS =?9
```

```
FREQ. (MHZ) =? .06
FREQ. (MHZ) =? .096
FREQ. (MHZ) =? .1
FREQ. (MHZ) =? .104
FREQ. (MHZ) =? .106
FREQ. (MHZ) =? .1065
FREQ. (MHZ) =? .107
FREQ. (MHZ) =? .1075
FREQ. (MHZ) =? .108
```

FREQ. (MHZ)	ATTENUATION (DBS)
.06	1.79854221362
.096	1.76130677777
.1	1.71308167581
.104	1.49871359025
.106	1.03198046146
.1065	.8
.107	512123192928
.1075	214094359849
.108	01956004902

```
IF REDESIGNING IS DESIRED FEED 1 OTHERWISE FEED 0. ?0
```

IdeasForDesign

and

$$\alpha = \ln(1+Z) = \frac{1}{2} \left[\ln \left[\frac{(F/(F-1))^2 + y^2}{(1/(F-1)^2 + y^2)} \right] \right]$$

where $F = \exp \alpha_0$.

The product $L_1 C_1$ is determined by f_0 , the pole position (see frequency profile of Fig. 1a). Resistor R_2 is equal to the dual of R_1 . The values of L_2 and C_2 are the dual of C_1 and L_1 , respectively.

The calculation procedure is similar for equalizers used with bandpass filters. The exception requires specification of an additional attenuation point, α_2 , at frequency f_2 (see curve in Fig. 1b). The equalizer's admittance function is then

$$y(s) = [(L_1 + L_2)C_1 s^2 + 1] / [L_1 s(L_2 C_1 s^2 + 1)]$$

The pole position, f_0 , determines the product of $L_2 C_1$.

The reference frequency should lie between the filter's lower passband edge, f_{p1} , and its minimum attenuation frequency, f_z . Reference frequency f_2 should be between f_z and the filter's upper passband edge, f_{p2} . The value of components L_1 and L_2 are determined from the admittance function, $y(s)$ evaluated at f_1 and f_2 respectively. The remainder of the components, R_2 , C_2 , L_3 , and C_3 , are the duals of R_1 , L_1 , C_1 , and L_2 , respectively.

In all cases actual component values are obtained by multiplying all resistor and inductor values by the required image impedance, $Z = R$, and dividing the capacitor values by R .

The program will specify the equalizer's response at any number of frequencies, given that $\alpha =$

Program for an equalizer for a 108-kHz low-pass filter

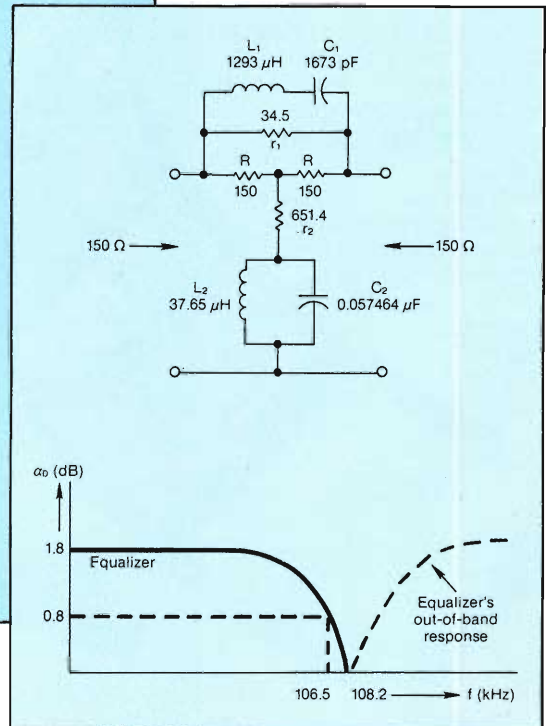
```

RUNNH
JOB: SAMPLE RUN (EQUALIZER FOR A 108 KHZ LOW PASS FILTER)
-----
TERMINATING IMPEDANCE(OHMS) =7150
TYPE OF FILTER- LOW PASS & HIGH PASS (1); BAND PASS (2):?1
-----
BASIC ATTENUATION (DBS) =?1.8
POLE POSITION (MHZ)=?1.082
REFERENCE FREQ.(MHZ) AND ATTENUATION (DBS)=?1.065;.8
R1= 34.5398297202      R2= 651.421856513
L1= 1292.95179484     C1= 1.37341686679E-03
L2= 37.6518795027    C2= .057464524214
TUNING FREQ.(MHZ) OF L1C1 & L2C2 = .1082
ALL RESISTORS ARE IN OHMS,
CAPACITORS ARE IN MICROFARADS AND INDUCTORS ARE IN MICROHENRIES
-----
ANALYSIS OF THE DESIGN OBTAINED :
-----
NO. OF FREQUENCIES FOR ANALYSIS =?9
FREQ.(MHZ)=?0.06
FREQ.(MHZ)=?0.096
FREQ.(MHZ)=?0.1
FREQ.(MHZ)=?0.104
FREQ.(MHZ)=?0.106
FREQ.(MHZ)=?0.1065
FREQ.(MHZ)=?0.107
FREQ.(MHZ)=?0.1075
FREQ.(MHZ)=?0.108

FREQ.(MHZ)           ATTENUATION(DBS)
.06                   1.79854221742
.096                  1.76130677777
.1                    1.71338167881
.104                  1.49871359025
.106                  1.03198046146
.1065                 .8
.107                  .512123192928
.1075                 .214094359949
.108                  .01836004902

IF REDESIGNING IS DESIRED FEED 1 OTHERWISE FEED 0 :?0
    
```

2. The program above calculates the component values of a bridged-T network that provides virtually uniform response over a low-pass filter's entire passband of dc to 108 kHz.



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$1n(1+Z)$. If the equalizer's attenuation characteristic does not meet the required response, the input parameters can be altered slightly and the network redesigned.

A complete listing of the program is given in Table 1, and a sample run for an equalizer using a 108-kHz low-pass filter is shown in Table 2. Resistor R_2 in the example can be connected to a tap on inductor

L_2 to increase the equalizer's Q . If center-tapped, L_2 should be increased to approximately 150 μH and capacitor C_2 reduced to 0.014366 μF .

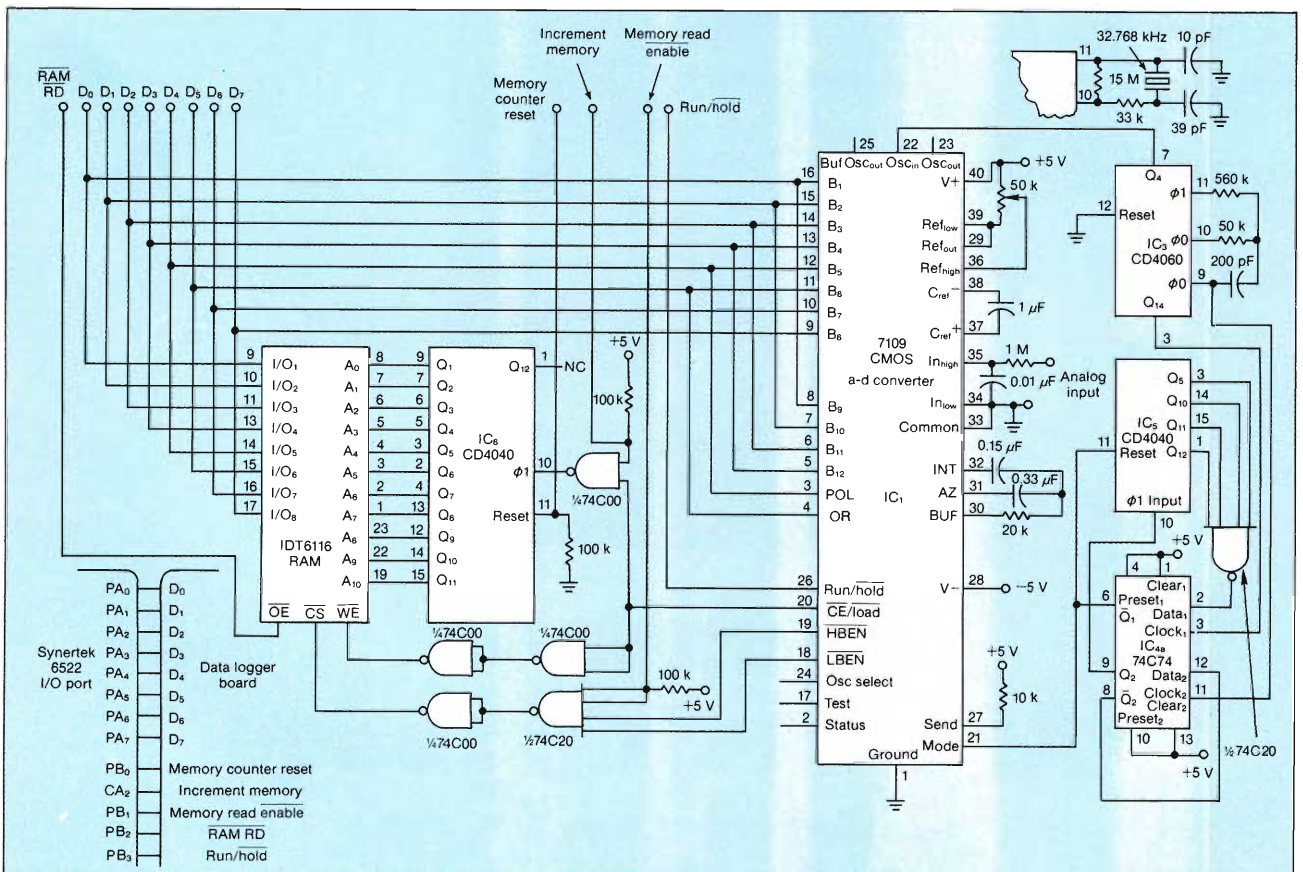
A. K. Goyal, Executive Engineer; C. Rao Kasarbada, Deputy General Manager, Research & Development Division, Indian Telephone Industries Ltd., P.O. Box 97, Naini, Allahabad-211010, Uttar Pradesh, India.

Stand-alone logger records 1024 bytes of 13-bit data

An analog-to-digital converter, a CMOS static RAM, and some gates and counters form a low-cost, flexible, stand-alone data-logging system that operates for weeks in remote or hostile environments. All the ICs are CMOS types and the clock frequency is low; thus the power supply drain is low enough to allow extended operation of the logger

from small on-board batteries.

The logger stores a 13-bit conversion (12 bits plus sign) in two consecutive bytes of memory. Because the time interval between measurements is programmable, the unit can make repetitive measurements over extremely long periods of time. For example, one 13-bit measurement can be made each hour for



An inexpensive yet reliable data logger stores up to 1024 bytes of 13-bit data at remote sites or in unattended laboratory experiments. Data gathered by the 7109 analog-to-digital converter is periodically clocked into a RAM for storage and retrieval by a computer. Because all parts are CMOS, battery drain is 15 mW.

READER FEEDBACK

Problems and proposals

We sincerely appreciate seeing our high-speed comparators put to work ["Modification Widens Comparator's Output Swing," July 7, 1983, p. 145]. However, we see some potential problems with Mr. Zaccai's proposed circuit:

1. When pin 3 falls to -10 V, it is still 25 V away from $+V_s$ and is thus still in violation of the LM319's 18-V absolute maximum rating (ground below $+V_s$).

2. Many LM319s will swing ± 10 V in the circuit shown, but not all of them. Some will swing ± 10 V at room temperature but will slow down and swing less to-

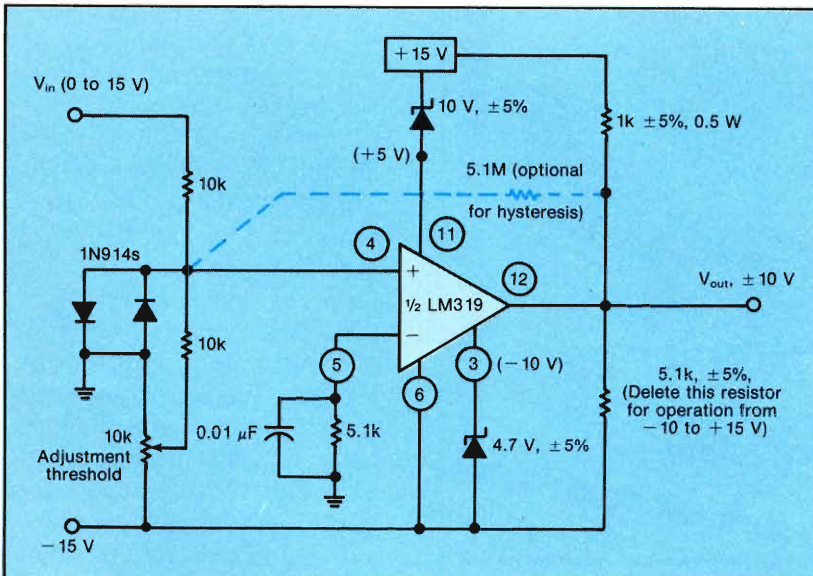
ward the negative as they warm up. The circuit is a little marginal in that respect.

3. The circuit causes the output transistors to saturate when pin 3 is near $+11$ V, in turn causing a delay of 150, 250, or 350 ns.

4. The capacitor on pin 4 will be charged up to a false value if V_{in} is more than 1 V away from threshold. When V_{in} returns to null, pin 4 will not be where the user thinks it is.

We believe that our circuit is a better approach: speed and accuracy are preserved. Further, no ratings are violated.

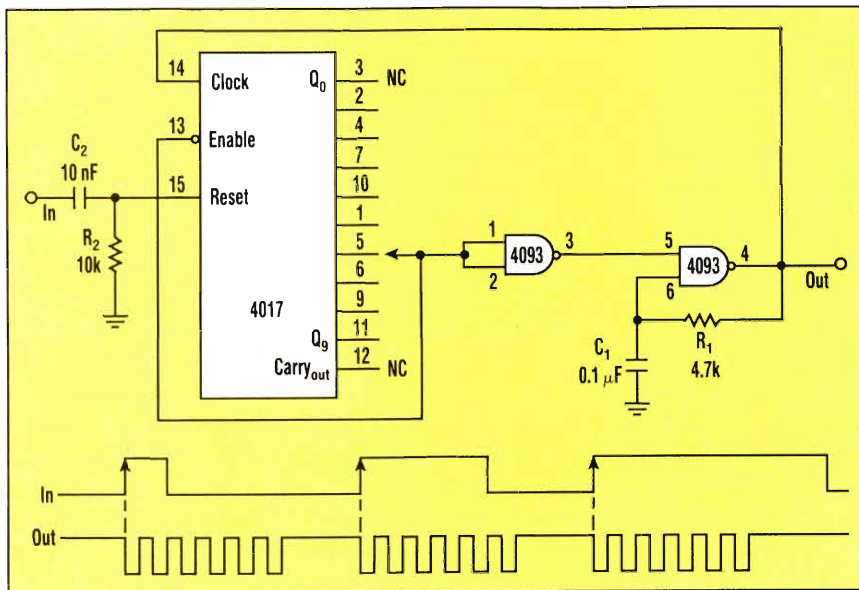
Robert A. Pease
Staff Scientist
National Semiconductor
Corp. Santa Clara, Calif.



CIRCLE 521 GET PULSE TRAIN FROM ONE PULSE

ELIAS ELIOPOULOS

117 Konstantinoupoleos, GR-132 31 Petroupoli, Greece.



THIS RATE-MULTIPLIER CIRCUIT contains a 4093 Schmitt trigger that acts as an oscillator, toggling the circuit's output (pin 4). The oscillator's pulses are then counted by the 4017 decade counter.

A rate-multiplier circuit can be used where one pulse must produce a pulse train, as in frequency multiplication, data sampling, etc. The circuit

was originally designed to convert the digital readout of an optical tachometer from revolutions/s to revolutions/min. It produces six pulses, but can be configured to generate a

predetermined number of pulses for every input pulse. The circuit's advantage over frequency multipliers using a phase-locked loop and dividers is that phase loss doesn't occur at the stabilization of the pulse train. This trait is especially useful when sampling asynchronous data signals.

One NAND Schmitt trigger (1/4 4093) acts as an oscillator (see the figure). When pin 5 goes low, the output stays high. When pin 5 goes high, the gate starts to oscillate with a free-running frequency:

$$f_{OSC} = R_1 \times C_1 \times \ln\left\{\frac{[V_{T+} \times (V_{DD} - V_{T-})]}{[V_{T-} \times (V_{DD} - V_{T+})]}\right\}$$

where V_{T+} and V_{T-} are the positive- and negative-going threshold voltages for the 4093. Their values can be found in the manufacturer's databook for the corresponding V_{DD} value.

When a positive-going pulse arrives at the In input, the 4017 decade counter is reset, output 0 goes high, and the decoded outputs 1 through 9 go low. The oscillator starts running and its pulses are counted by the 4017. The 4017's outputs go high sequentially until the sixth pulse. Then, the oscillator is inhibited and its output remains high, waiting for the next triggering pulse. To configure the circuit to produce between 1 and 9 pulses, tie pins 1 and 2 of the 4093 to the appropriate 4017 output. □

CIRCLE 522 QUALITY PREAMP CUTS COST, SIZE

WALT JUNG and RICHARD MARKELL

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900.

To achieve low noise and 600-Ω (or less) load capability, traditional recording-studio mixing panels use high-cost modular or hybrid amplifiers with matched input-stage transistors and push-pull A-B outputs. Though the expected high performance is achieved, the solution is large and expensive. An alternative approach uses a low-input-noise audio op amp added to a high-quality class-A buff-

er amp. The resulting circuit forms a variable-gain, transformer-coupled microphone preamp. The preamp is equal to the discrete design in performance, and superior in cost, size, and overall complexity.

IC U_1 is a low-noise LT1115 audio op amp that's operated in a class-A mode by J_1 , a 2-mA current source (Fig. 1). U_1 's output is buffered by U_2 , an LT1010 buffer amp. U_2 can be adjusted to supply a class-A stand-

IDEAS FOR DESIGN

ing current by the 49.9- Ω resistor at the Boost pin, and is capable of very low open-loop distortion.¹ U_3 , an LT1097 precision op amp, is configured as a dc servo to null output offsets that can cause distortion in the output transformer, T_2 . T_1 is carefully selected to match R_n , the LT1115's characteristic noise resistance.² Both transformers should be properly shielded and grounded for optimum performance in this low-level application.

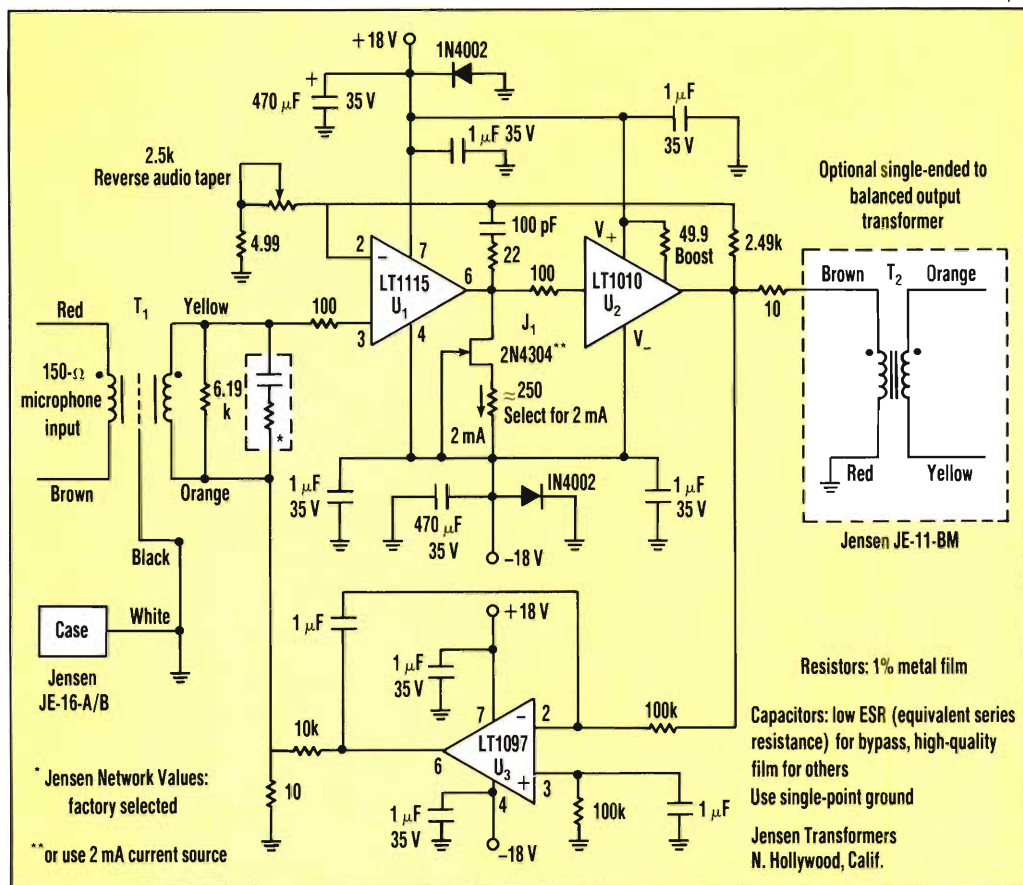
Using the gain control, the circuit's overall gain can be adjusted from 12 to 50 dB. The distortion and frequency-response, plotted at an operating gain of 20 dB, illustrate the circuit's performance (Fig. 2). The risetime of the preamp approximates the Bessel response characteristic, now favored by specialists in the audio field. For top performance, the circuit should be operated with well-bypassed, low source-impedance power supplies. □

¹Jung, W.G., R.N. Markell, "Low

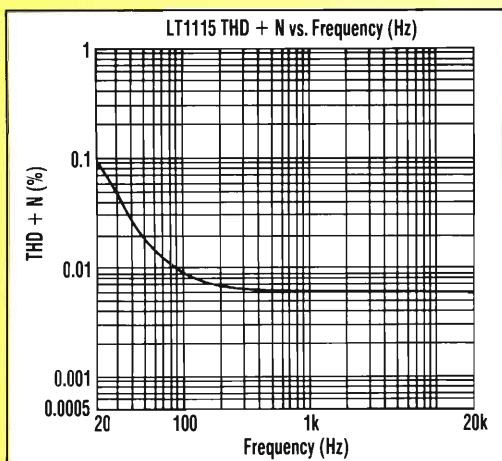
Distortion Video Buffer," *ELECTRONIC DESIGN*, March 9, 1989.

²Jung, W.G., *Audio IC Op-Amp*

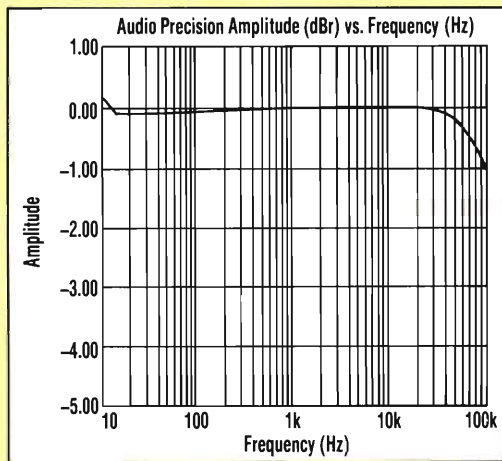
Applications, Third Edition, Howard W. Sams and Co., Indianapolis, Ind., 1987.



1. A LOW-INPUT NOISE AUDIO OP AMP (LT1115) is coupled with a class-A buffer amp (LT1010) to form a variable-gain, transformer-coupled microphone preamp. By altering the gain control, the circuit's overall gain can be adjusted from 12 to 50 dB.



$V_s = \pm 18 \text{ V}$
 $V_{in} = 0.95 \text{ V rms}$
 $R_L = 600 \Omega$
 $R_S = 150 \Omega$
 $T_A = 25^\circ \text{C}$

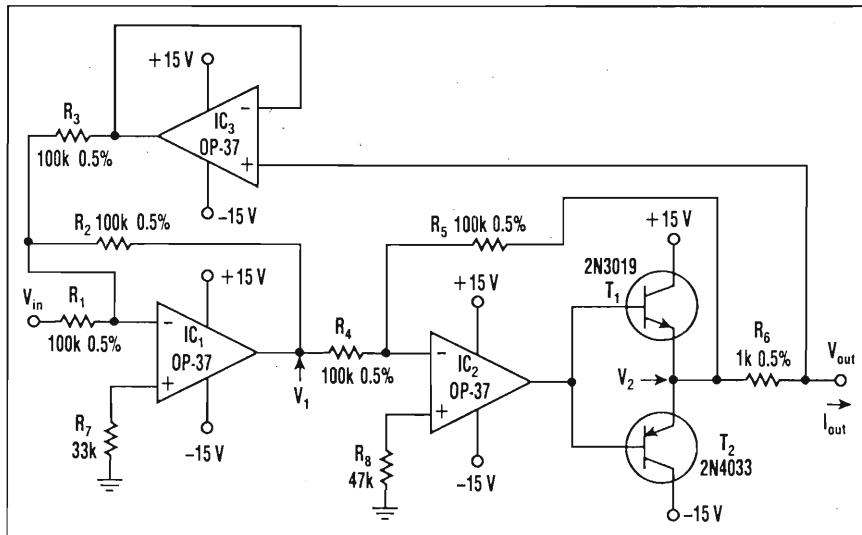


2. THE CIRCUIT'S TOTAL HARMONIC DISTORTION (THD) plus noise is plotted against frequency (a). A second plot shows the circuit's frequency response (b). Both plots illustrate an operating gain of 20 dB with a balanced input-output.

CIRCLE 523 GROUND LOAD WITH V/I CONVERTER

FRANTISEK MICHELE

Barvicova 17A, CS 60200 Brno, Czechoslovakia.



THIS VOLTAGE-TO-CURRENT CONVERTER has many advantages, such as working into a grounded load, high precision, and simple control of the I_{out}/V_{in} ratio.

This voltage-to-current converter circuit is beneficial in many analog applications. The circuit, which consists of three op amps, two medium-power transistors, and a few passive components, has many advantages over alternative circuits (*see the figure*). These include load-grounding possibilities, simple control of the I_{out}/V_{in} ratio, high precision, linearity, stability, bandwidth, and low noise. It also has an I_{out} range from about $1 \mu A$ to the maximum I_C of T_1 and T_2 and an output resistance of about $50 M\Omega$.

Op-amp IC_1 inverts the sum of V_{in} and V_{out} :

$$V_1 = -(V_{in} + V_{out}).$$

IC_2 and T_1 and T_2 invert V_1 :

$$V_2 = -V_1 = -(- (V_{in} + V_{out})) = V_{in} + V_{out}.$$

Then, to calculate the output current I_{out} :

$$I_{out} = (V_2 - V_{out})/R_6 = (V_{in} + V_{out} - V_{out})/R_6 = V_{in}/R_6.$$

This formula shows that the value of I_{out} depends only on V_{in} and R_6 .

Voltage follower IC_3 reduces the current from the circuit's output to the input of IC_1 by a sufficient amount so that this current's influence can be neglected. □

CIRCLE 521 ATTAIN DRIVE FOR MOSFET RELAY

DAVID JOHNSON

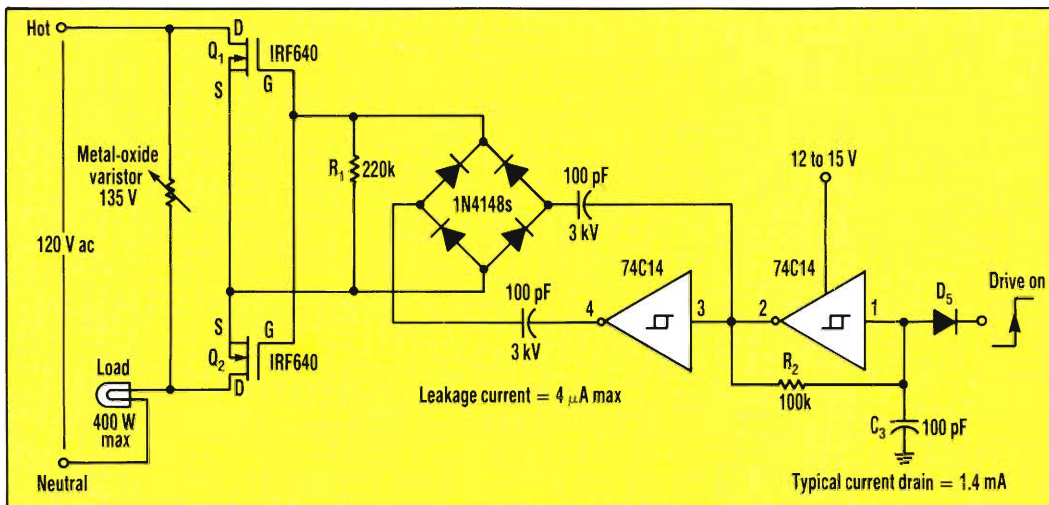
10198 W. Berry Dr., Littleton, CO 80127; (303) 973-8408.

The necessary drive for a MOSFET bidirectional relay, used to switch power to 120-V ac loads, can be supplied by a circuit where two CMOS Schmitt triggers (74C14) form a 100-kHz square-wave oscillator with complementary outputs (see the figure). The two output signals are cou-

pled to the FET gates of the relay circuit through a pair of 100-pF capacitors and a bridge rectifier that converts the ac voltage to dc. Sufficient gate-source capacitance within the FETs eliminates the need for any added filtering.

Resistor R_1 's value (220 k Ω) is chosen to discharge the capacitance and

turn the transistors off in about 2 ms once the drive signal has been disabled. Faster switching times are possible using lower values of R_1 and higher drive frequencies. With the values shown, less than 2 mA of current is needed from a 12- to 15-V supply to drive the circuit. In addition, with such a small coupling capacitance, the leakage current from the power line to the CMOS driver circuit is less than 5 μ A, which is sufficient isolation for many applications. Leakage currents less than 1 μ A are possible by using a 1-MHz drive frequency and 12-pF coupling capacitors. \square



TO SUPPLY the drive needed for a MOSFET bidirectional relay, the Schmitt triggers (74C14) form a 100-kHz square-wave oscillator with complementary outputs. The outputs are rectified bridge and applied to the FET gates of the relay circuit. R_1 turns off the transistors.

CIRCLE 522 CONVERT V_C TO DUTY CYCLE

B. STASICKI

Max Planck Institut für Strömungsforschung, Göttingen, W. Germany; (0551) 709-1.

A voltage-to-duty-cycle converter can be useful in many applications such as pulse-forming networks. This externally-triggered circuit generates a rectangular TTL (high-speed CMOS) signal with a duty cycle that's a linear function of the control voltage (V_C). The period of the TTL signal is given by the trigger frequency, f_{in} . The duty cycle is frequency independent over a wide range.

The circuit consists of a positive-edge triggered monostable multivibrator (U_1) and an analog integrator (U_2) (Fig. 1). U_1 , from an HC or HCT family, generates rail-to-rail pulses of duration t_w , controlled by the collector current of Q_1 . The duty cycle of U_1 's output equals $t_w \times f_{in}$.

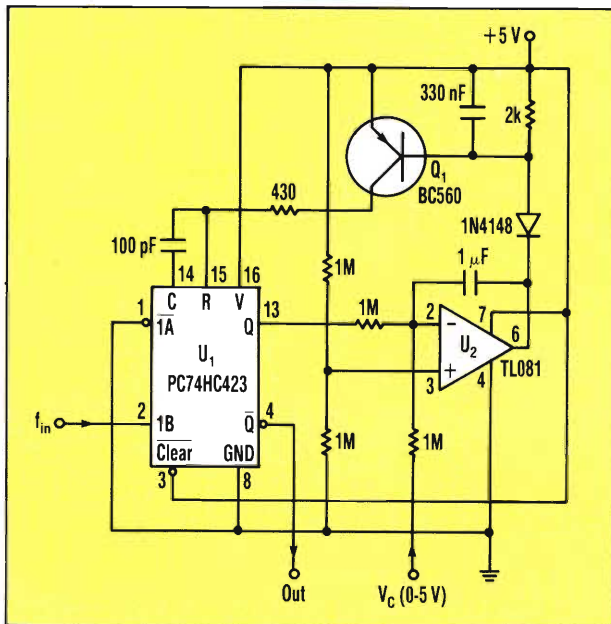
The mean value of a rectangular signal is proportional to its duty cycle. As a result, U_2 will supply an error signal for the feedback loop. This signal controls U_1 's output-pulse

width, t_w , keeping the duty cycle at a constant value given by the control voltage, V_C , where

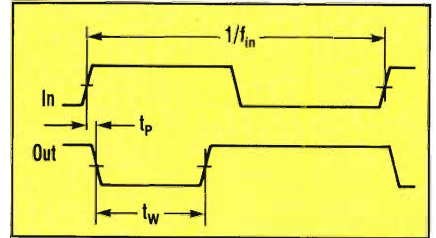
$$\text{duty cycle} = 1 - V_C/5.$$

To get a duty cycle directly proportional to the control voltage, add an analog inverter that supplies $5V - V_C$.

The circuit is powered by a +5-V supply. Because this voltage is also used as a reference, it must be stable to obtain good voltage-to-duty-cycle-conversion accuracy. With the components specified in figure 1, the converter is stable and accurate in the range from 100 Hz to above 1 MHz. The settling time for large and fast V_C changes is about 1 second. The upper-frequency limit is due to the minimum pulse width t_{wmin} (50 ns) that can be generated by a multivibrator and the multivibrator recov-



1. THIS circuit converts voltage to duty cycle by taking the output of a monostable multivibrator (U_1) and sending it through an integrator (U_2). The integrator then supplies a signal that controls U_1 's output-pulse width, keeping the duty cycle at a constant value (V_C).



2. AT HIGH frequencies, when the circuit is used as a voltage-to-phase-shift converter, propagation-delay time (t_p) must be considered. The shift caused by t_p can be avoided if a negative-output transition is used as a reference.

$$\phi(\text{degrees}) = 360(1 - V_C/5).$$

Therefore, the circuit can also be used as a frequency-independent voltage-to-phase converter for TTL trigger signals. The operating frequency and phase-shift ranges correspond to those obtained when the circuit is used as a voltage-to-duty-cycle converter. However, at higher operating frequencies, the additional phase shift caused by the propagation delay time, t_p (40 ns), must be considered (Fig. 2). If the application uses the negative output signal transition as a reference for phase shift instead of a positive-input-signal, this shift will be avoided. □

ery time t_R (30 ns). The lower limit depends on the integrator R-C parameter. To maintain stability, the R-C parameter should be much greater than $1/f_{in}$. But a higher R-C value increases the circuit's settling time.

For a given value of f_{in} , the lowest duty cycle is determined by t_{wmin} and the highest by t_R . For example, when $f_{in} = 10$ kHz, the minimum duty cycle is $50 \text{ ns} \times 10 \text{ kHz} = 0.0005$ and the

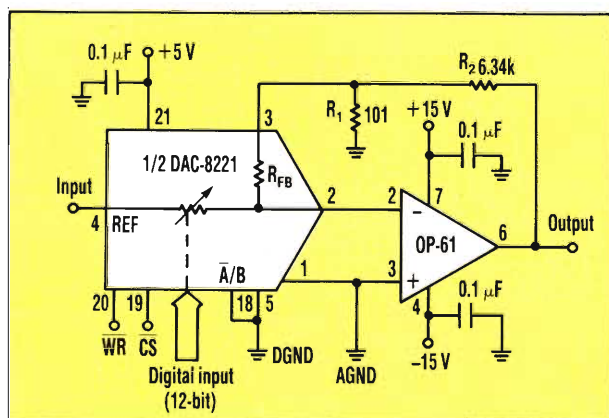
maximum is $1 - 30 \text{ ns} \times 10 \text{ kHz} = 0.9997$. However, the operation at extremely high duty cycle values isn't recommended, because the multivibrator can be retriggered due to the pulse-width jitter effect in this region and the output pulse missed.

Note that the positive-output signal transition is shifted by the phase (ϕ) relative to the positive-input-signal transition, where

CIRCLE 523 ADD PROGRAMMABLE GAIN, ATTENUATION

JAMES WONG

Analog Devices, Precision Monolithics Div., 1500 Space Park Dr., PO Box 58020, Santa Clara, CA 95052; (408) 727-9222.



1. BY adding R_1 and R_2 in the feedback loop around a DAC, the circuit functions as a digitally-programmable amp. The gain or attenuation is variable over the range of $1/64$ to 64 . The resistors are connected in a T-configuration.

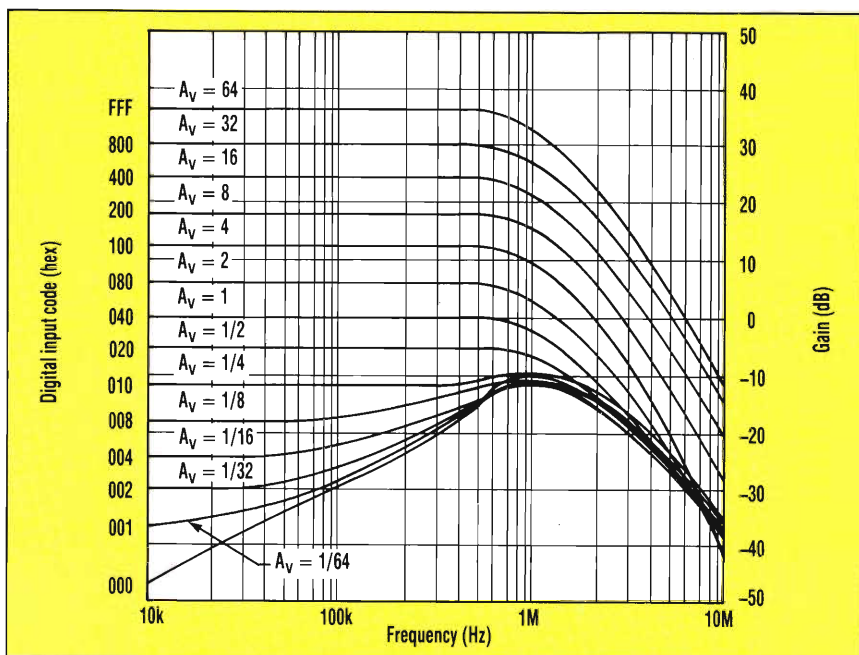
By adding two resistors to the output-amp feedback loop of a current-output digital-to-analog converter (DAC), both gain control and attenuation control can be achieved (Fig. 1). This digitally programmable amplifier produces gain and attenuation in the range of $1/64$ to 64 . The circuit gets its range from a 12-bit CMOS DAC.

The design works because the transfer function from the DAC's input to its output is purely voltage at-

attenuation. Connecting R_1 and R_2 in a "T" configuration inside the output amp's feedback loop produces a voltage gain from the resistor junction to the output. If R_1 is much less than R_{FB} (11 k Ω in this example), the gain produced nearly equals $1 + (R_2/R_1)$, or 64. The result is a programmable gain amp with a transfer function of $A_V = -(D/4096)(64)$,

where D represents the DAC's binary-weighted digital code. Of course, the added gain of the T-network increases the circuit's noise gain. Therefore, it's important to choose first a low-noise amplifier.

By using a low-noise, high-frequency op amp, such as the OP-61, the circuit will have a wide bandwidth performance even at high gain settings. The circuit's frequency response can be plotted at different gain settings (*Fig. 2*). At high gains, the amp has a 1-MHz bandwidth. \square



2. GAIN IS PLOTTED versus frequency for various digital inputs of the DAC. The amplifier has a 1-MHz bandwidth at high gains, but it drops for gains below 1/4.

CIRCLE 523 OP AMP REGULATES ITS OWN SUPPLY

M.S. NAGARAJ

ISRO Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore 560017 India.

To function properly, analog comparators and their potential dividers that provide reference voltages should be powered by well-regulated supplies. In many cases, quad comparators or quad op amps used as comparators are operated in single-supply mode and are energized by three-pin regulator ICs.

A quad comparator or op amp and its associated circuits can be powered by a precision supply with a

line regulation of better than 0.05%. This is done by adding a transistor, a Zener diode, and a few resistors to one of the four amps on the same IC. It's also possible to trim the precision power-supply voltage.

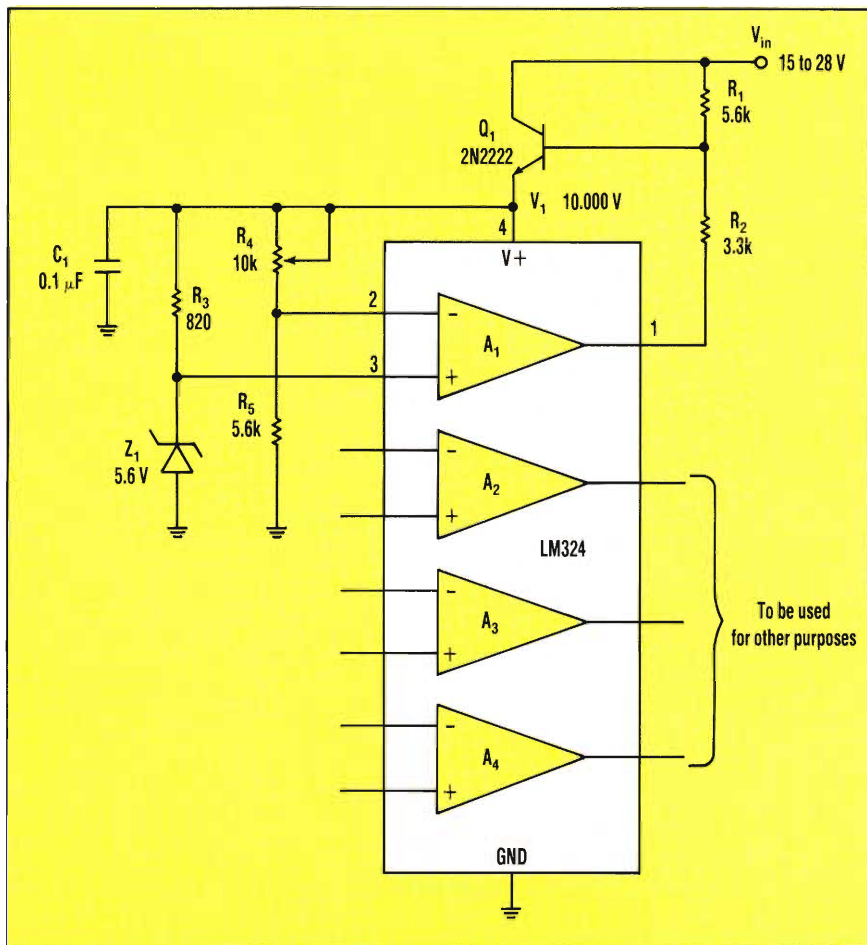
This op-amp circuit offers a straightforward method of developing a single-polarity stable voltage source (see the figure). Transistor Q_1 gets a base drive through resistor R_1 , and conducts to develop a voltage (V_1) across the IC's supply pins. Amp

Correction: In the November 22 Ideas for Design section, Fig. 2 for "Derive Stable dc from ac Current" should have had a connection from the cathode of D_2 to the bottom of C_1 .

A_1 , R_2 , and Q_1 form a positive-feedback closed loop along with R_3 and the Zener diode. A_1 , R_2 , and Q_1 also form a negative-feedback closed loop with R_4 and R_5 . The effect of positive feedback is predominant as the noninverting input receives V_1 while the inverting input receives only $V_1 \times [R_5/(R_4 + R_5)]$. This happens until the Zener comes into play. When the voltage at the inverting input exceeds the voltage at the noninverting input, A_1 's output takes away Q_1 's base current through R_2 , reducing V_1 . Hence, an equilibrium condition is reached. Now,

$$V_1 = V_Z(R_4 + R_5)/R_5.$$

When tested in practice, V_1 was trimmed to 10.000 V and stayed at that value for an input voltage variation from 15 to 28 V. Besides energizing the IC, it was also determined that the circuit can source 30 mA, which is more than enough to energize the potential dividers. It's also enough to drive control circuits, such as relay and lamp drivers associated with other amps on the same IC. □



ONE OP AMP on this quad op-amp IC regulates the reference voltage for the whole chip. A_1 , along with a transistor, a Zener diode, and a few resistors can precisely supply the chip's reference voltage, even when V_{in} varies from 15 to 28 V.

CIRCLE 521 DRIVE 100-MA CABLE LOADS

JIM WILLIAMS

Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035; (408) 954-8400.

Capacitance or cable loads with currents of 100 mA can be driven by an amplifier circuit that has over 20 MHz of small-signal bandwidth. The circuit's input capacitance is below 1.5 pF, bias current is about 100 pA, and the output is fully protected. These features make this amplifier suitable for use as an automatic-test-equipment (ATE) pin amplifier, a video analog-to-digital converter input buffer, or a cable driver. The circuit also permits wideband probing when oscilloscope probing isn't tolerable. The overall amplifier consists of a low-input capacitance FET, two LT1010 buffers, and a gain stage— Q_3 and Q_4 (Fig. 1).

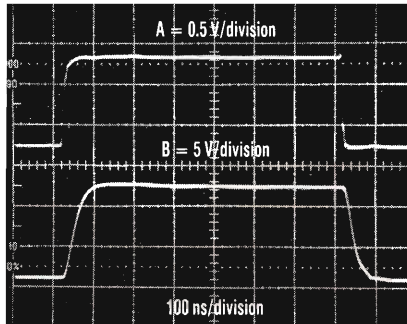
A_3 acts as a dc restoration loop. The 33- Ω resistors sense A_1 's operating current, biasing Q_3 and Q_4 . These devices furnish complementary voltage gain to A_2 , which supplies the circuit's output. Feedback is from A_2 's output to A_1 's output, which is a low impedance point. The "current-mode" feedback permits fixed bandwidth over a wide range of closed-loop gains. This contrasts with typical feedback schemes where bandwidth degrades as closed-loop gain increases.

A_3 's stabilizing loop compensates for large offsets in the signal path, which are dominated by a mismatch in transistors Q_3 and Q_4 . A_3 measures the dc difference between the amplifier's input and its output and biases

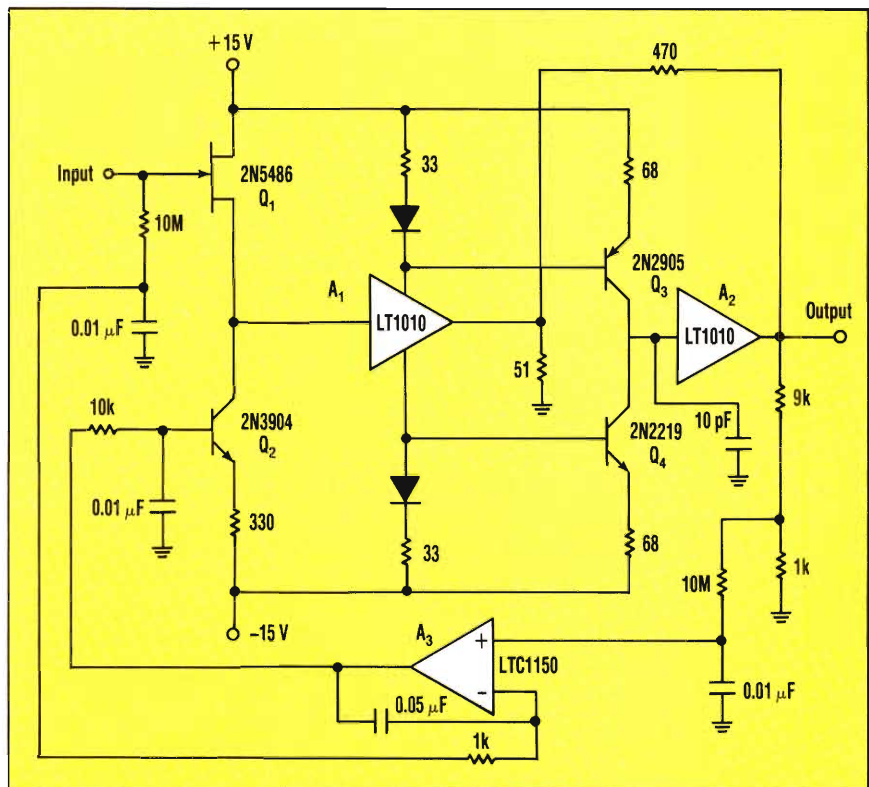
the signal path to correct for offset. Correction is implemented by controlling Q_1 's channel current through Q_2 . The channel current sets Q_1 's V_{GS} , enabling A_3 to control overall circuit offset. The 9- to 1-k Ω divider that feeds A_3 is selected to equal the gain ratio of the circuit, in this case 10.

The feedback scheme makes A_1 's output look like the amplifier's negative input, with closed-loop gain set by the ratio of the 470- and 51- Ω resistors. The outstanding feature of this connection is that the bandwidth becomes relatively independent of closed-loop gain over a reasonable range. For this circuit, small-signal bandwidth exceeds 20 MHz over gains of 1 to 20. The loop is quite stable, and the 10-pF value at A_2 's input supplies good damping over a wide range of gains.

Large signal performance can be seen at a gain of 10 when driving 10 ft. of cable (Fig. 2). The response displayed at the output is quick and clean and has no slew residue or poor dynamics. □



1. WITH 20 MHz of small signal bandwidth, this circuit can drive 100-mA capacitance or cable loads. The circuit's feedback, from A_2 's output to A_1 's output, permits a fixed bandwidth over a wide range of closed-loop gains.



2. INPUT PULSE A produces output pulse B. These signals are for an amplifier gain of 10, driving 10 ft. of cable.

IFD WINNER

IFD Winner for September 27

David Johnson, 10198 W. Berry Dr., Littleton, CO 80127; (303) 973-8408. His idea: "Convert Waveform Period To Voltage."

CIRCLE 522 CONTROL RF SIGNALS DIGITALLY

MICHAEL A. WYATT

SSO Honeywell Inc., Clearwater, FL 34624; (813) 539-5653.

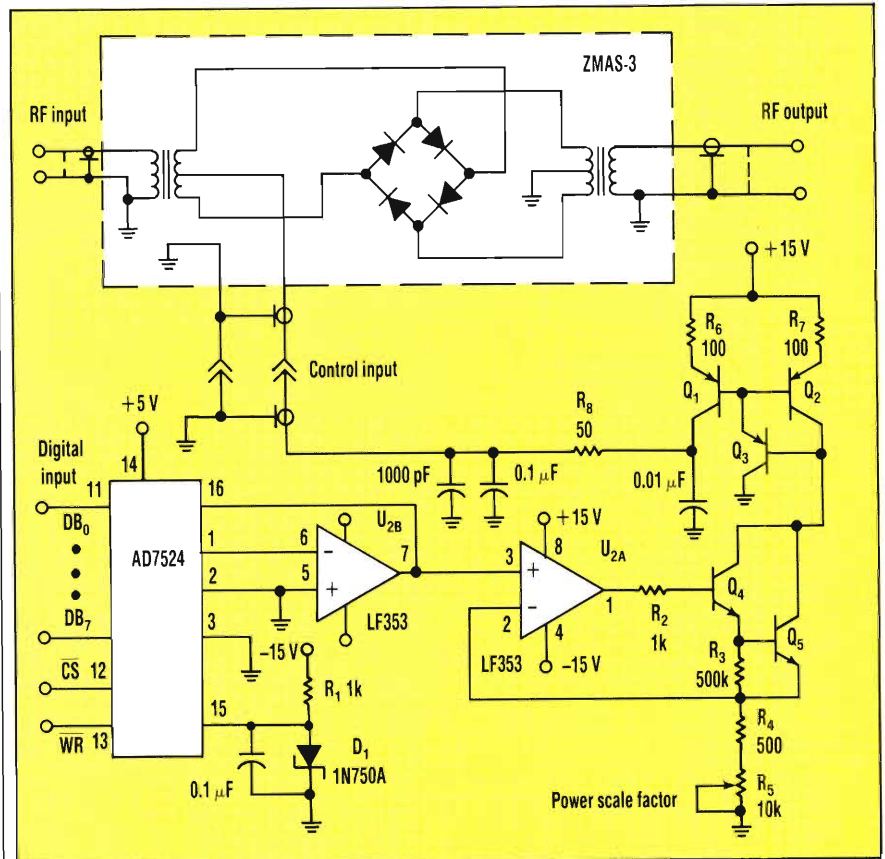
high and the attenuation needed. This can be used in a lookup table or curve-fit to an equation. If a greater attenuation range is required, the attenuator sections should be cascaded and a dual DAC, such as the AD7528, should be used. □

By combining a balanced mixer, voltage-controlled current source, and a digital-to-analog converter, a digitally controlled radio-frequency attenuator can be produced (*see the figure*). The mixer (ZMAS-3), specifically designed for attenuator operation, acts as a current-controlled transmission gate between the RF input and output ports. Current enters the control input and forward biases the quad diode array within the mixer. Because the diodes' conductance is proportional to forward current, the transmission of RF energy from the RF input to the output flows through the diode array and is thus controlled by the diode array's forward current. The mixer's control range is over 40 dB within a frequency range of 1 to 200 MHz. Other ranges are available from its manufacturer, Mini-Circuits, Brooklyn, N.Y.

Transistors Q_{1-5} , along with op amp U_{2A} , form a voltage-controlled current source. These transistors can be any general-purpose devices, such as 2N3904s, 2N3906s, or part of an array, such as the CA3096. Potentiometer R_5 sets the attenuator's scale factor by establishing the voltage-to-current transfer ratio.

The AD7524 8-bit DAC from Analog Devices, Norwood, Mass., supplies the overall digital control by producing a digitally selected voltage that drives the voltage-controlled current source. The digital input is an 8-bit word that uses CS and WR to latch the data into the DAC.

To calibrate, R_5 is adjusted with the DAC at its maximum value (all bits high) to establish the minimum attenuation. Then, the DAC is set to its minimum value (all bits low) to establish the maximum attenuation. The difference between the maximum and minimum attenuation is the attenuator's control range. Each DAC bit can now be sequentially set



THIS RADIO-FREQUENCY ATTENUATOR, which is digitally controlled, combines a balanced mixer, a voltage-controlled current source, and a digital-to-analog converter. The DAC produces a digitally selected voltage that drives the current source. R_5 sets the attenuator's scale factor.

CIRCLE 523 ADD SENSING TO LM317 REGULATOR

M. S. NAGARAJ

ISRO Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore 560 017 India.

Though they're convenient to use, three-terminal regulators can't sense and correct for a voltage drop across the conductors carrying the load current. An optocoupler helps perform

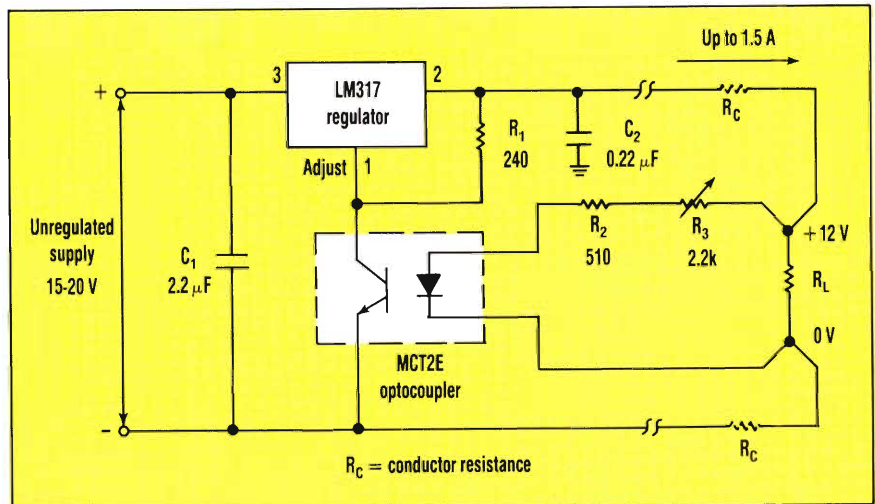
the sense function (*see the figure*).

Setting R_1 to 240 Ω causes a 5-mA constant current to flow through the optocoupler's transistor. R_3 is adjusted to achieve the desired 12 V across the load. A voltage drop

IDEAS FOR DESIGN

across the load caused by a larger drop in the conducting path lowers the current through the optocoupler's light-emitting diode. This action drives the transistor toward its "off" state and increases its V_{CE} . Hence, the regulator's Adjust and output voltages increase until the load voltage reaches the nominal value of 12 V.

The process is reversed when the voltage drop across the conductor decreases. Note that the nonlinearity in the optocoupler response is accounted for by the negative feedback built into the circuit. □



BY USING AN OPTOCOUPLER with a three-terminal regulator, this circuit corrects for voltage drops across the conductors carrying the load current. When the load voltage falls due to an increased I_R drop through the conductors, the current through the optocoupler's light-emitting diode is reduced, driving the transistor toward cutoff and increasing its V_{CE} voltage. This raises the LM317's Adjust voltage, which keeps the load voltage steady at 12 V. Should the I_R drop across the conductors decrease, the opposite action takes place.

CIRCLE
521 GET NEGATIVE RAIL USING CMOS GATES

DAVID CUTHBERT

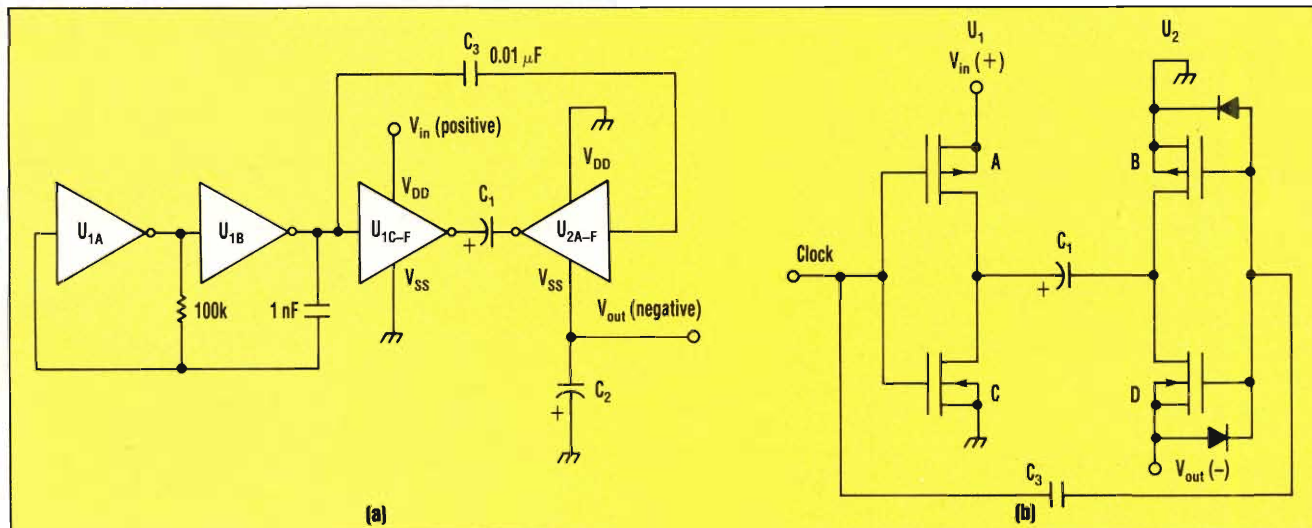
Tektronix Inc., TV Waveform Displays Div., M.S. W3 100, P.O. Box 500, Beaverton, OR 97077.

By implementing this inexpensive circuit built with CMOS gates, a negative rail can be obtained from a positive supply. The circuit's input range is 1.2 to 7.0 V, and the no-load loss is only 1 mV. The negative rail can be generated from one 1.5-V cell.

Two 74HC04 CMOS hex inverter chips are used in a charge-pump circuit (see the figure, a). Two gates from U₁ form a 7-kHz clock oscillator. The four remaining gates are paralleled for the positive side of the pump. All six gates in U₂ are paralleled for the negative side of the

pump (see the figure, b). When the clock is low, FETs A and B are on and C₁ is charged to V_{in}. When the clock is high, C and D are on. C₁'s positive end is grounded while its negative end is connected to the circuit's output. The clock signal is coupled to the input of U₂ through C₃. U₂'s input-protection diodes clamp the signal to ground, creating a dc bias across C₃.

The converter output impedance is about 100 Ω and the maximum output current is 10 mA. With an input of 1.5 V, the no-load supply current is 20 μA. With C = C₁ = C₂, the peak-to-peak output ripple equals V_{in}/2RFC. □



A NEGATIVE RAIL IS OBTAINED from a positive supply by using two 74HC04 CMOS hex inverter chips in a charge-pump circuit (a). In the simplified circuit, C and D are configured so that when the clock is high, the positive end of C₁ is grounded while the negative end is connected to the output (b).

CIRCLE
522 SPICE2 MODELS BJT BREAKDOWN

DONALD B. HERBERT

26284 Via Desmonde, Lomita, CA 90717.

Avalanche-breakdown phenomena in bipolar junction transistors has been characterized in literature for a long time.^{1,2} The multiplication factor (M) is commonly used to formulate the increase in collector current at or near avalanche breakdown, where:

$$M = 1/[1 - (V_{CB}/V_A)^N].$$

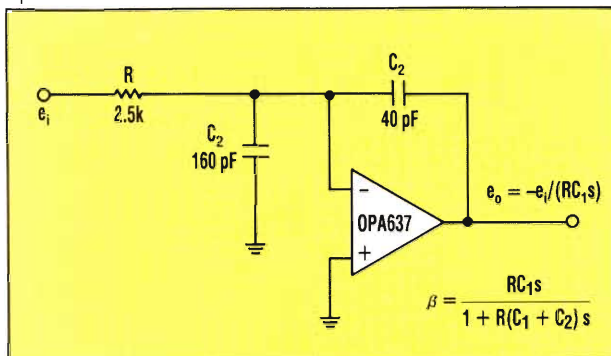
In this equation, V_{CB} represents the applied collector-base voltage, V_A is the avalanche-breakdown voltage, and N is the breakdown rate. N is an adjustable index depending on material constants and geometrical factors; for a silicon pn junction, N is about 3.

The application of the M factor can be extended with a Spice2 implemen-

tation. This is useful to study transistor operation in the vicinity of avalanche breakdown in various circuit configurations.

The multiplication factor can be added to a Spice2 bipolar transistor model in the form of a controlled current source connected from collector to base with a current equal to (M - 1) × I_C (Fig. 1). This is similar to a previously published approach.¹ Consequently, the added current source implements a total equivalent collector current equal to M × I_C, which reduces to I_C at V_{CB} voltages well below avalanche breakdown.

In Spice2, the augmented transistor model can be implemented with



BY ADDING a capacitor (C_2), the integrator feedback factor stays below unity. Thus, higher-slew-rate op amps which are phase compensated for gains greater than unity can be employed.

and supplies a slew rate of $135 \text{ V}/\mu\text{s}$ (see the figure). The equivalent unity-gain stable OPA627 has a slew rate of only $55 \text{ V}/\mu\text{s}$. To deliver the higher slew rate to the integrator, the circuit is modified by adding C_2 .

Without C_2 , the typical integrator encounters a short-circuit feedback through C_1 . At high frequencies, the capacitor's low impedance effectively shorts the feedback path, producing a unity feedback factor. Feedback factor is simply the fraction of the output voltage fed back to the op-amp input. Without C_2 , this voltage-divider ratio becomes unity when C_1 's impedance is very low compared to resistor R .

Adding C_2 alters the high-frequency feedback factor to reduce the op-amp phase-compensation requirement. With C_2 , the voltage-divider ratio between op-amp output and input is reduced. At higher frequencies, C_1 's low impedance no longer competes only with R 's fixed impedance. Now, R is bypassed by C_2 to counteract the dominance otherwise produced by C_1 's falling impedance. As frequency increases, R 's significance is still removed, but C_2 retains the voltage-divider action. Ultimately, the high-frequency feedback factor becomes $C_1/(C_1 + C_2)$; this factor is easily made less than unity. Then, the op amp employed needn't be unity-gain stable. The higher slew rate version of the op amp is accommodated by the integrator circuit without concern for frequency stability.

The op amp shown supplies a 2.5:1 improvement in the slew rate available to the integrator. In practice, integrator slewing isn't pushed to the op amp's slew-rate limit. When an op

amp is rate limited, the amplifier introduces large errors. To counteract this, integrator slewing is set below the amplifier limit by hand picking the feedback elements. For the components shown, a 10-V level for e_i produces a 4-mA current in the resistor. This current is delivered to C_1 where charging causes e_o to slew at $de_o/dt = e_i/RC_1 = 4 \text{ mA}/40 \text{ pF} = 100 \text{ V}/\mu\text{s}$. As a result, the slew rate demanded from the amplifier is below its limit of $135 \text{ V}/\mu\text{s}$ and accurate integrator response is retained. However, this slew rate demand is above the $55 \text{ V}/\mu\text{s}$ available from the unity-compensated version of the amp.

Adding C_2 doesn't alter the circuit's basic integrator response. Input signal e_i is impressed on R to develop the feedback current e_i/R . This current reacts with C_1 's impedance to produce an output voltage of $-e_i/(RC_1 s)$. Consequently, the output voltage continues to reflect the input signal's integral. Because e_i isn't impressed on C_2 , this capacitor doesn't affect the integrator circuit's basic input-to-output response.

Adding C_2 , however, will incur bandwidth and noise consequences and excessive C_2 capacitance should be avoided. Closed-loop bandwidth decreases and noise gain increases as the feedback factor is reduced. The best choice for C_2 sets the maximum feedback factor for the minimum stable gain of the amplifier. Then, frequency stability is assured and the bandwidth and noise degradation is minimized. The maximum feedback factor, β_{max} , meets the optimum condition when:

$$1/\beta_{\text{max}} = (C_1 + C_2)/C_1 = A_{\text{min}}$$

Here, A_{min} is the minimum gain for stable operation of the op amp. From

the above expression, the optimum C_2 is defined as:

$$C_2 = (A_{\text{min}} - 1)C_1.$$

With this choice of C_2 , only noise performance is compromised for the higher slew rate. C_2 decreases the bandwidth, but from a higher starting point. The reduced phase compensation that requires the reduced feedback factor actually increases amplifier bandwidth. The lesser-compensated amplifier delivers the same bandwidth at A_{min} that the greater compensated version offers at unity gain. Amplifier noise, however, increases with the higher slew-rate option. The op-amp input noise is amplified by $1/\beta$. At higher frequencies, adding C_2 increases noise gain from unity to $1/\beta_{\text{max}} = (C_1 + C_2)/C_1$.

At first, it seems that frequency stability is also compromised by adding C_2 . This capacitor supplies a return to ground for C_1 , resulting in a capacitive load on the op amp's input. The load is $C_L = C_1 C_2 / (C_1 + C_2)$. Still, this load is small due to practical limitations. As described above, an integrator's output slewing is also limited by the integrator feedback. In practice, any integrator that approaches the op-amp slew rate has a relatively small value for C_L . □

IFD WINNER

**IFD Winners for
November 22, 1990**

Gary Kath and Sandy Hobbs,
Sharp & Dohme Research Laboratories,
P.O. Box 2000, R80-A18,
Rahway, NJ 07065; (201) 594-5225.
Their idea: "Create Control-Panel Labels."

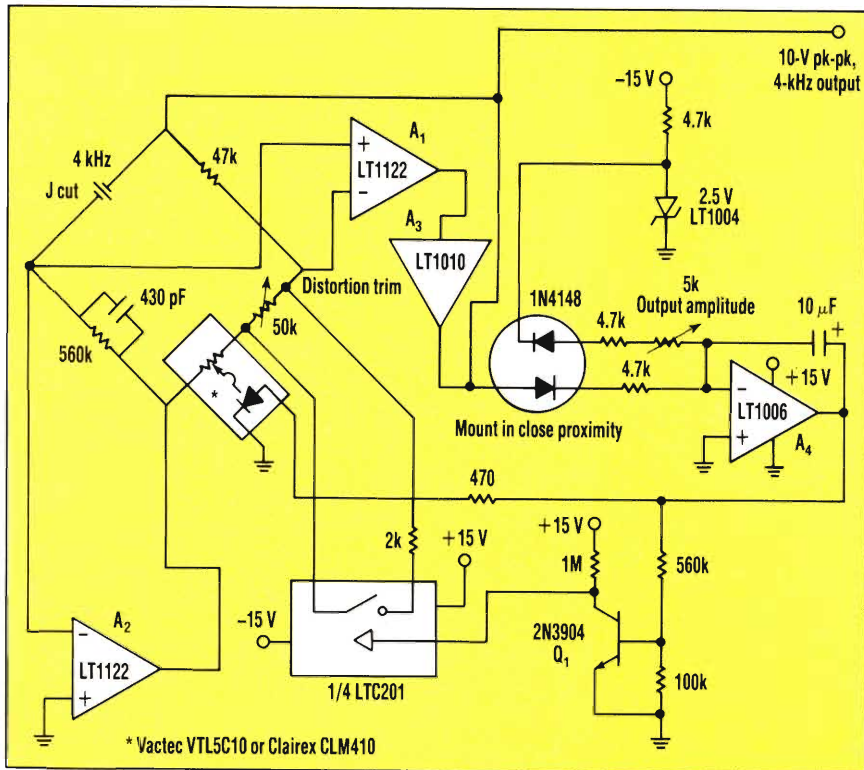
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CIRCLE 521 DISTORTION STAYS UNDER 9 PPM

JIM WILLIAMS

Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035; (408) 954-8400.



* Vactec VTL5C10 or Clairex CLM410

1. A LOW-DISTORTION OUTPUT is generated by this quartz-stabilized oscillator circuit. The 50-kΩ potentiometer is adjusted for minimum distortion while monitoring A₃'s output with a distortion analyzer.

Data-converter, audio, and filter testing often require a spectrally pure sine-wave oscillator. This quartz-stabilized oscillator circuit supplies a stable frequency output with extremely low distortion (*Fig. 1*). The 4-kHz oscillator has less than 9 ppm (0.0009%) distortion in its 10-V pk-pk output.

To understand the circuit's operation, temporarily assume that op amp A₂'s output is grounded. With the crystal removed, A₁ and the power buffer (A₃) form a noninverting amplifier with a grounded input. The circuit's gain is set by the ratio of the 47-kΩ resistor to the 50-kΩ potentiometer-photoresistor pair. Inserting

the crystal closes the positive feedback path at the crystal's resonant frequency. This causes oscillation to occur.

A₄ compares A₃'s positive peaks with the LT1004 2.5-V negative reference. The diode in series with the LT1004 supplies temperature compensation for A₃'s rectifier diode. A₄ biases the LED portion of the photoresistor's resistance. As a result, loop gain is set to a value that permits stable

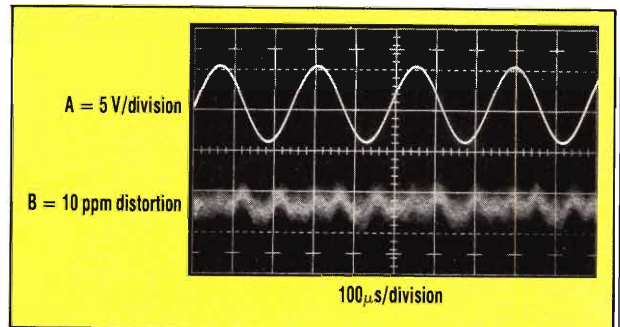
amplitude oscillations. The 10-μF capacitor stabilizes this amplitude-control loop.

A₂ eliminates the common-mode swing seen by A₁. This dramatically reduces distortion due to A₁'s common-mode rejection limitations. A₂ does this by servo-controlling the 560-kΩ photoresistor junction to keep its negative input at 0 V. Common-mode swing is thus eliminated at A₁, leaving only the desired differential signal.

Transistor Q₁ and the LTC201 switch form a startup loop. When power is first applied to the circuit, oscillations may not occur or they may build very slowly. Under these conditions, A₄'s output saturates positive. This turns Q₁ on. The LTC201 switch turns on, shunting the 2-kΩ resistor across the 50-kΩ potentiometer. This raises A₁'s loop gain, forcing a rapid buildup of oscillations. When the oscillations rise high enough, A₄ comes out of saturation, Q₁ and the switch go off, and the loop functions normally.

The circuit is set for minimum distortion by adjusting the 50-kΩ potentiometer while monitoring A₃'s output with a distortion analyzer. This trim sets the voltage across the photoresistor to the optimum value for lowest distortion.

After trimming, A₃'s output contains less than 9 ppm distortion (*Fig. 2*). Residual distortion components include noise and third-harmonic residue. Oscillation frequency, set by crystal tolerance, is typically within 50 ppm, with less than 2.5 ppm/°C drift. □



2. THE 10-V PK-PK OUTPUT OF A₃ has a distortion that's less than 9 ppm (trace A). The residual-distortion components include noise and third-harmonic residue (trace B).

to charge through the 100-kΩ resistor. Once the capacitor charges past the threshold voltage of the second input (pin 3), the triac is activated. This enables the circuit to act as a voltage doubler.

If the ac line voltage is greater than 146 V ac, the output of channel 1 (pin 6) is activated, pulling channel

2's input below its threshold. The triac is then turned off, making it possible for the input diodes to perform as a full-wave bridge (Fig. 2).

This circuit has two unique features. First, the circuit is powered by negative supply. This enables the triac to be activated in two of its more sensitive quadrants (quadrants 2

and 3), thus lowering the current requirement of the circuit. Second, only the negative half cycles are sensed, which could create a problem. However, because a delay is needed during power up to prevent the circuit from prematurely going into voltage-doubler mode, a time delay already exists. □

CIRCLE 522 IC GENERATES NONINTEGRAL POWERS

ROBERT S. VILLANUCCI

Wentworth Institute of Technology, 550 Huntington Ave., Boston, MA 02115; (617) 442-9010.

By using a circuit built with an analog multiplier and two potentiometers, an output voltage (V_0) can be made to approximate the input voltage raised to the power of n (V_x^n) (Fig. 1). The value of n can be any nonintegral power between 1 and 2. The circuit comes in handy when a nonlinear sensor's output requires algebraic curve fitting. In addition, it can be scaled for the correct output-voltage level and calibrated for law conformity with just two resistor adjustments.

The circuit implements a series approximation that states:

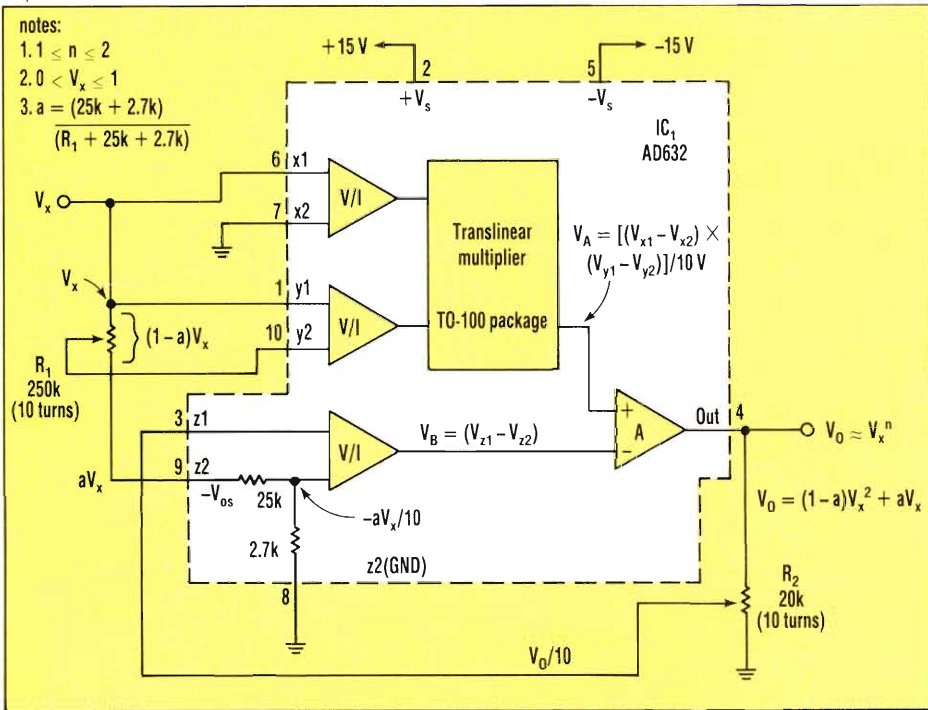
$$V_0 \approx V_x^n = (1-a) \times V_x^2 + aV_x.$$

Here, a is the resistor-divider ratio between IC₁'s internal 2.7-k to 25-kΩ network and R_1 's setting. To create the approximation, start with the transfer function for the IC:

$$V_0 = (V_{x1} - V_{x2}) \times (V_{y1} - V_{y2}) = 10 \text{ V} \times (V_{z1} - V_{z2}).$$

Substitute 0 V for V_{x2} and $(1-a)V_x$ for the difference voltage, $V_{y1} - V_{y2}$. Then, remove IC₁'s 10-V scale factor by creating $V_0/10$ on R_2 's wiper and applying it to the $z1$ input. The approximation is completed by using the internal network at $z2$ to create the term $aV_x/10$.

The circuit's output voltage can be seen when it's superimposed on a 1-V peak positive triangle-wave input, and n is set to 1.6 (Fig. 2). Scale the nonintegral power generator by setting the input to its maximum value (1 V), then adjust R_2 until $V_0 = 1$ V (1 raised to any power equals 1). To calibrate for law conformity, raise a convenient value of V_x , say 0.4 V, to the value of n . With n set to 1.6 in this



1. WITH JUST an analog multiplier and two potentiometers, V_0 can approximate V_x^n , where n equals any nonintegral power between 1 and 2. The circuit can be scaled for the correct output voltage and calibrated for law conformity by adjusting R_1 and R_2 .

2. THE circuit's output waveform is superimposed onto its input. In this case, n is set to 1.6. It shows that $V_x^n \approx V_0$.

n	a	R ₁ (setting)
1.0	1.00	0
1.2	0.72	38.47k
1.4	0.45	61.56k
1.6	0.30	92.34k
1.8	0.16	173.13k
2.0	0.00	∞

← Short R₁ (for n=1.0)
 ← Remove R₁ (for n=2.0)

circuit, $V_0 \approx 0.4^{1.6} \approx 0.231$ V. Adjust R_1 until the output equals 0.231 V. The values of R_1 vary from 0, when $n = 1$, to infinity, when $n = 2$ (see the table). □

Reference:

Analog Devices Inc. "AD632 Internally Trimmed Precision IC Multiplier" data sheet. Norwood, Mass., July, 1982.

CIRCLE 523 SELECT SERIES OR PARALLEL COMBO

JON VICKLUND

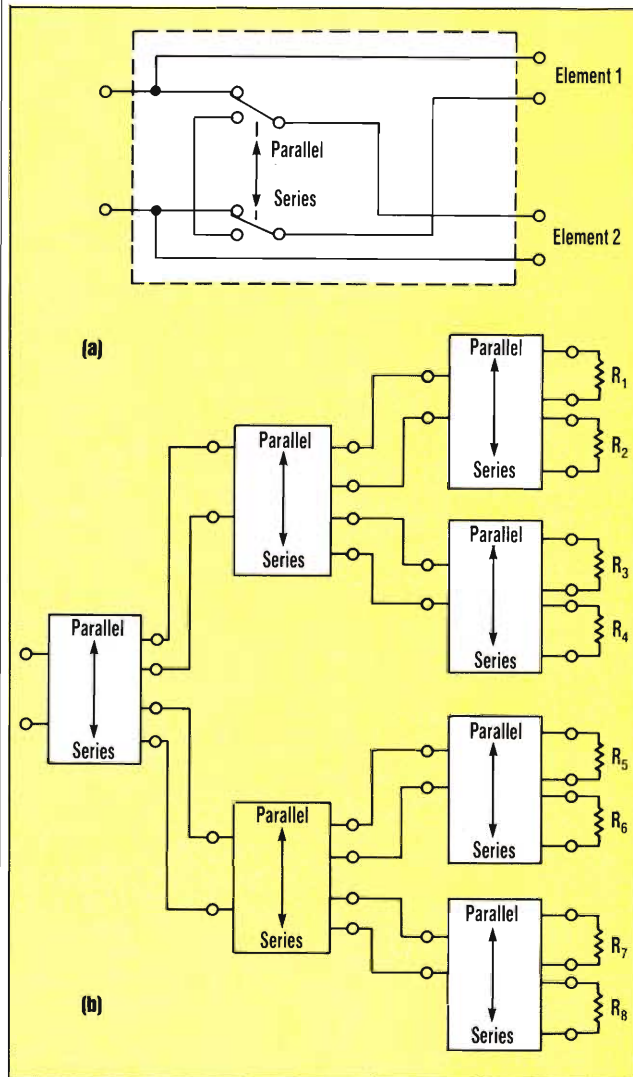
Ball Aerospace, P.O. Box 1062, Bldg. FA-2, Boulder, CO 80306; (303) 939-4496.

With a DPDT switch or relay, users can select either the series or parallel combination of any

two elements (see the figure, a). The elements used in the circuit can be any two-terminal device, such as a resistor, a capacitor, an inductor, or a

battery or solar cell. Polarized as well as nonpolarized elements can also be used. The direction of the current within the element is the same regardless of which position the switch occupies.

If several switches are ganged together, a load box is created (see the figure, b). This load box is very flexible, supplying loads for high-voltage, low-current sources when all the switches are in series or low-voltage, high-current sources when all the switches are in parallel. There are 2^n combinations of loads, where n equals the number of DPDT switches or relays employed. Using different values for resistors R_{1-8} will avoid having repetitive combinations. □

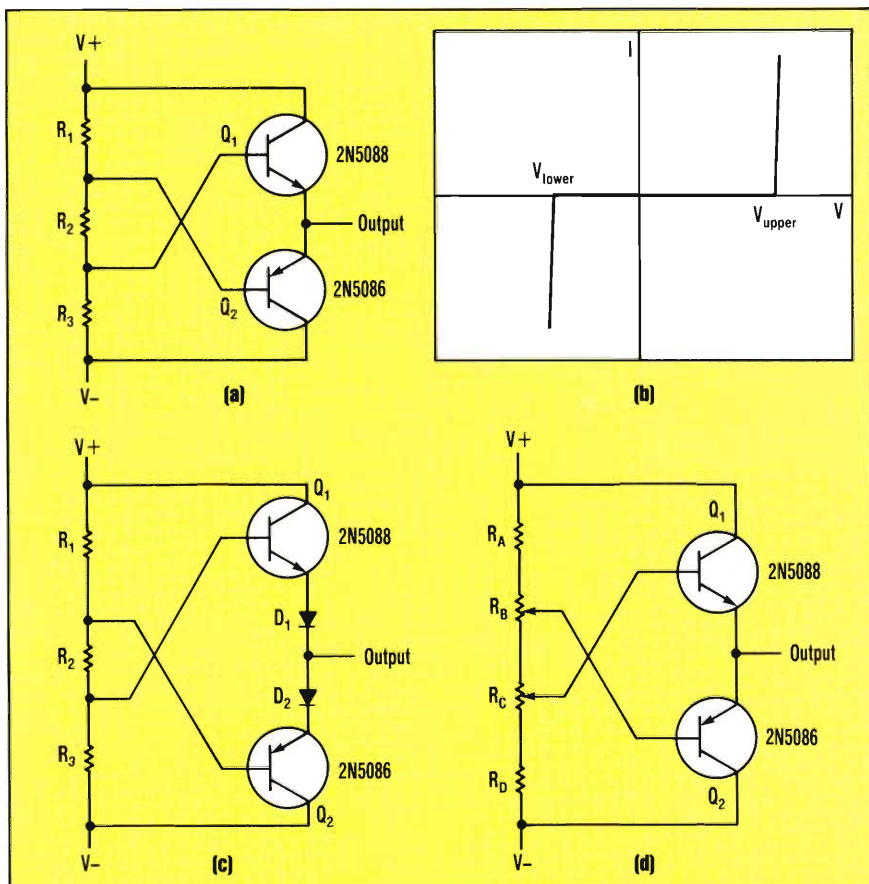


EITHER A SERIES OR A PARALLEL combination of any two, two-terminal devices can be selected by correctly configuring this circuit (a). By ganging several of the switches together, a load box can be created (b). The box supplies the loads for high-voltage, low-current sources (series) or low-voltage, high-current sources (parallel).

CIRCLE
521 VOLTAGE LIMITER
IS ADJUSTABLE

MICHAEL J. ENGLISH

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.



THIS CIRCUIT LIMITS SIGNAL LEVELS to specific amplitudes without using Zener diodes (a). The circuit's V-I characteristic resembles a circuit containing Zeners connected back-to-back (b). Adding two diodes removes the 8-V pk-pk limitation (c). By replacing the three resistors of the original circuit (a) with two fixed resistors and two potentiometers, users can easily adjust the limiting level (d).

Signal levels must often be limited to specific amplitudes in various applications, such as test systems and pulse generators. Voltage limiting also plays an important role in input-overvoltage and electrostatic-discharge protection. This circuit functions as a programmable two-quadrant voltage limiter (see the figure, a).

The circuit's V-I characteristics resemble a pair of Zener diodes connected back-to-back (see the figure, b). This implementation's advantage is that the voltage limits can be set or adjusted to any level within the allowed signal range. The clipping levels aren't constrained to standard Zener voltages and tolerances.

The clipping levels are given by:

$$V_{upper} = V_- + (V_+ - V_-)(R_2 + R_3) /$$

$$(R_1 + R_2 + R_3) + V_{be}(Q_2) \text{ and}$$

$$V_{lower} = V_- + (V_+ - V_-)(R_3) /$$

$$(R_1 + R_2 + R_3) - V_{be}(Q_1).$$

The maximum peak-to-peak range between limiting levels must be less than the lowest BV_{ebo} of the transistors used. This is because the transistors' emitter-base junctions are reversed biased for signals between the limit values. For the devices shown, the limit is about 8 V pk-pk. This limitation in peak-to-peak range can be overcome using two diodes with higher breakdown voltages (see the figure, c). The clipping levels must be modified to include the diodes' added forward voltage drop.

Replacing R_1 , R_2 , and R_3 with two fixed resistors and two potentiometers allows simple level adjustment (see the figure, d). □

CIRCLE
522 KEEP SPICE ACCURACY
ABOVE 1 MHz

STEVEN C. HAGEMAN

Calex Mfg. Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523; (415) 932-3911.

Simple equivalent circuits of common discrete ceramic capacitors and film resistors can greatly enhance the accuracy of Spice simulations when frequencies exceed 1 MHz or the tran-

sient step interval is less than 1 μ s. One equivalent circuit is for a 1/4-W film resistor (Fig. 1a). The model includes shunt capacitance and equivalent series inductance (ESL) effects. The ESL and capacitance are more

products of the package size than resistor value, so the nominal values shown work for all values of 1/4-W composition or film resistors.

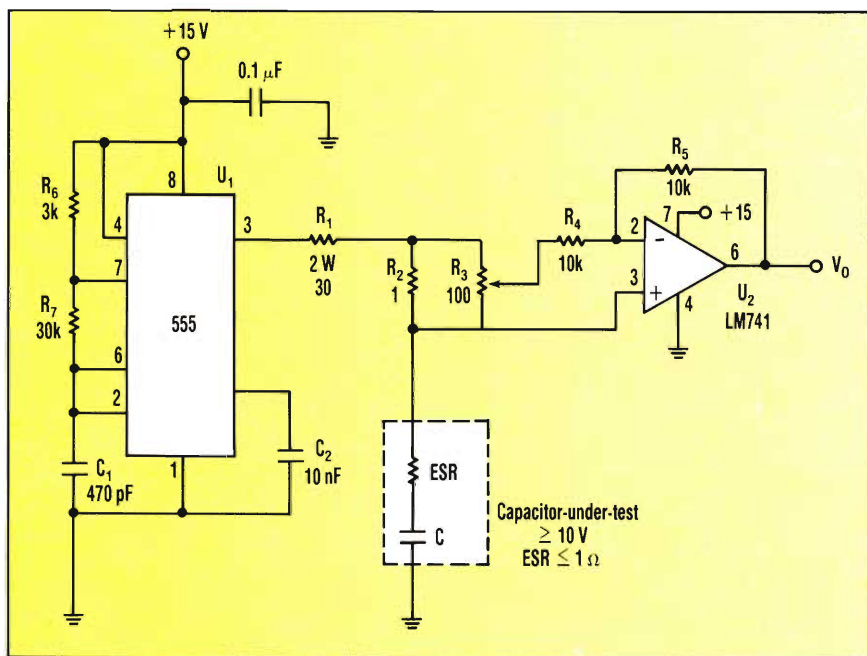
In a second circuit representing a ceramic capacitor, the ESL and equivalent series resistance effects are simulated (Fig. 2a). The nominal values given are good for small 100-pF types up to 0.2-in., 1- μ F square types, with little loss in accuracy. PSpice net lists are generated for the two subcircuits (Figs. 1b and 2b).

The impedance characteristics of

CIRCLE
521 MEASURE ESR
OF A CAPACITOR

CARL SPEAROW

Sundstrand Corp., 4747 Harrison Ave., Rockford, IL 61125; (815) 394-3263.



USING THIS CIRCUIT AND AN AC VOLTMETER, the equivalent series resistance of a capacitor can be measured. Adjust resistor R_3 until the output voltage is minimized. Multiply the value of the potentiometer by the value of resistor R_2 . Then, that product is the ESR.

The equivalent series resistance (ESR) of a capacitor can be measured using this circuit and an ac voltmeter (see the figure). U_1 functions as a 50-kHz square-wave generator. It drives a current waveform of about ± 180 mA in the capacitor-under-test through R_1 and R_2 . When R_3 is adjusted to the proper value, the voltage drop across the equivalent series resistor is precisely nulled by the inverting amplifier (U_2). Thus, V_0 is the pure capacitor voltage which is the minimum voltage that can be produced at V_0 .

To make an ac voltage measurement, adjust R_3 until V_0 is minimized. Then note the position of the potentiometer and multiply it by the value of R_2 , 1 Ω in this case. That product equals the capacitor's ESR. The capacitor is biased at about 7.5 V. Lower-voltage capacitors won't work with this circuit. By changing the value of R_2 , other ranges of ESR can be measured. However, for small R_2 values, the current level should be increased to keep a reasonable voltage across R_2 . This will require some sort of buffer. The circuit is intended for capacitors greater than 100 μ F. The ripple voltage gets large for smaller values and accuracy decreases. □

IFD WINNER

IFD Winner for
January 31, 1991

Jim Williams, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 954-8400. His idea: "Drive 100-mA Cable Loads."

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CIRCLE
522 FIND FILTER SETTLING
TIME WITH EASE

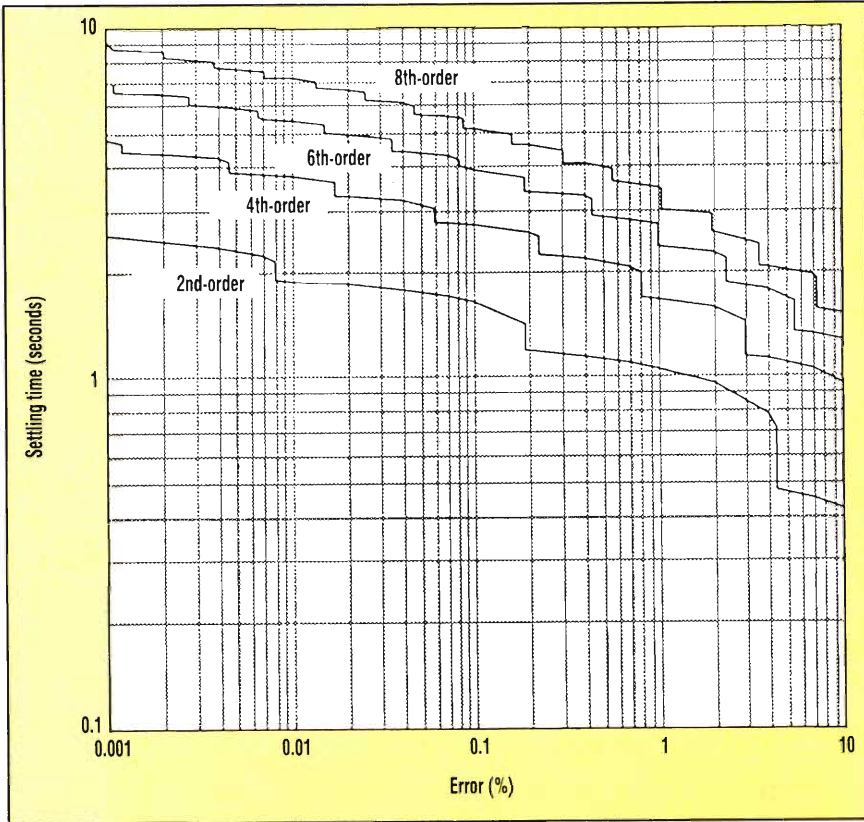
KERRY LACANETTE

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.

Anytime a filter is added to a system, its presence affects the system's transient response. This occurs whether it prevents aliasing in an analog-to-digital converter or reduces out-of-band noise at the front-end of an instrument. The filter's settling time depends on its order, its cutoff frequency, and the desired accuracy. Settling time is the time required for output to equal the input within a specified accuracy when the circuit is driven by a step input signal. De-

termining the settling time of an arbitrary filter analytically is tedious and is usually avoided by the prudent engineer.

The curves shown offer a quick way to find the settling time of a Butterworth low-pass filter with minimal calculation (Fig. 1). The percentage error to which the filter must settle is on the horizontal axis. The vertical axis shows the settling time for a low-pass filter with a 1-Hz cutoff (-3 dB) frequency. For filters with cutoff frequencies other than 1 Hz, sim-



For example, if the settling time to 1% error of a 1-kHz, 6th-order, Butterworth low-pass filter is needed, use the 6th-order curve. The 1% settling time of a 1-Hz filter is $t_{S1} = 2.7$ seconds. Dividing this result by 1000 (the value of f_c) gives the settling time for the 1-kHz filter—2.7 ms. For an LMF60 6th-order, switched-capacitor, Butterworth low-pass filter with an input voltage step of 4 V, the filter settles to 1% when the ringing amplitude is within 40 mV of the final value. This result agrees closely with the number obtained from the curve (Fig. 2).

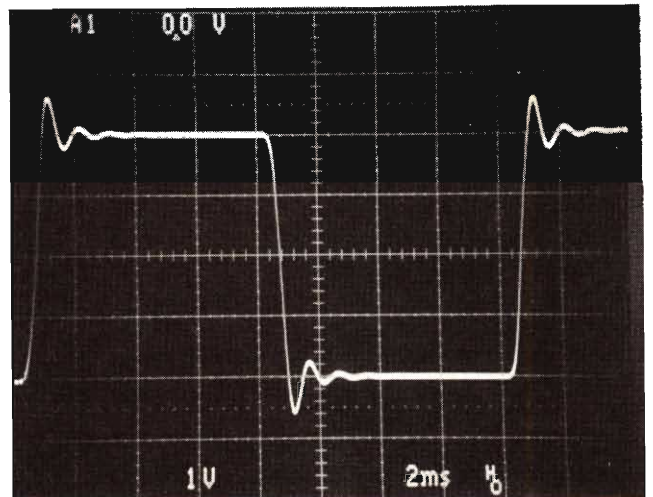
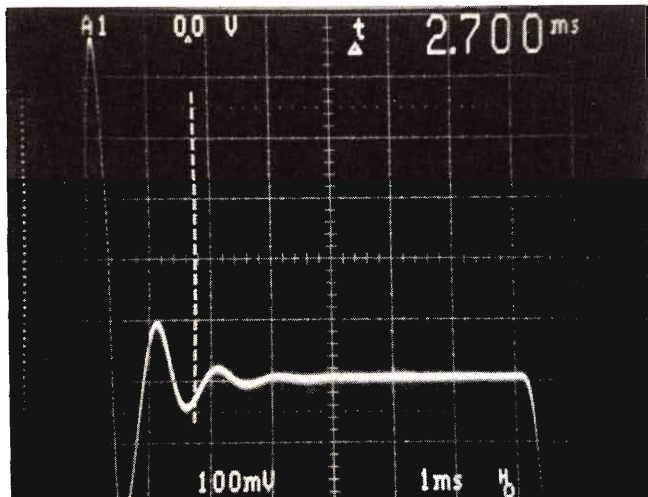
The discontinuous nature of the curves occurs because the step response of a Butterworth filter with an order greater than one exhibits ringing. Therefore, a given error can exist at several times. Consequently, a curve showing settling time versus error can't be smooth. For example, the step response of a 6th-order Butterworth filter settles to within 10% of the final value at about 1.26 ms (Fig. 2, again). Following the settling waveform from this point, the error decreases smoothly until about 5.52% is reached, which is the value of the error at the step response's first negative-going peak. The settling time then "jumps" from 1.34 to 1.64 ms for an error of 5.52%. Each peak or dip in the step response contributes an additional discontinuity in the settling-time-versus-error curve. □

1. THESE CURVES REPRESENT the settling time versus error for 2nd-, 4th-, 6th-, and 8th-order Butterworth low-pass filters with 1-Hz cutoff frequency. To find the settling time of a filter with a different cutoff frequency, divide the settling time obtained from the curve by the filter's cutoff frequency.

Simply divide the settling time obtained from the curve by the filter's cutoff frequency:

$$t_s = t_{S1}/f_c$$

where t_s represents the filter's settling time, f_c is the value of its cutoff frequency, and t_{S1} is the settling time of a 1-Hz filter as obtained from the curve.



2. THE STEP RESPONSE of an LMF60 6th-order Butterworth low-pass filter is displayed. The input step is 4 V and the settling time to 1% (40 mV) is about 2.7 ms as predicted by the curve.

Solving for t ,

$$t = -1/1.70 \ln(1 - V_c/13.3).$$

Q_1 turns on when V_c equals 3 V, which occurs about 150 ms after the supply's output reaches 4.5 V. Q_2 turns on at when V_c equals 7.4 V, which occurs about 330 ms later. These times are sufficiently long enough to ensure that the supply has time to stabilize and that Q_1 and Q_2 turn on slowly. Turning the FETs on slowly is critical because the startup current must be kept to a minimum. If the FETs are switched too fast, large current spikes can occur, defeating the purpose of the soft-start circuit.

There are penalties for adding the soft-start circuit. The circuit is considered to be part of the power supply, so power that's dissipated by the circuit hurts the supply's efficiency as a whole. Most of the power is lost due to the nonzero on-resistance of the output pass transistor (Q_2). The IRFD9210 has an on-resistance of 0.6 Ω . At an output current of 500 mA, Q_2 will dissipate 300 mW. If this loss is unacceptable, a FET with a lower on-resistance (and usually higher price) can be used.

The resistance across Q_2 also hurts load voltage regulation because the switching supply's voltage sense is taken from the transistor's input side. As long as the load current is relatively constant, this isn't a serious problem. If the variation in output voltage is unacceptable, load regulation can be improved by using a lower on-resistance FET. It can also be improved by adding a voltage-sense circuit on the output side of Q_2 , which can be enabled after the soft-circuit operation finishes. While the circuit shown should only be used with -48- to +5-V switching supplies, it can be modified for various switching-supply applications. \square

Send in Your Ideas for Design

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CIRCLE 523 BUILD A SIMPLE AMP COMPONENT

DON SCHEDEL

Motorola Inc., 8220 E. Roosevelt, P.O. Box 9040, Scottsdale, AZ 85252; (602) 441-6752.

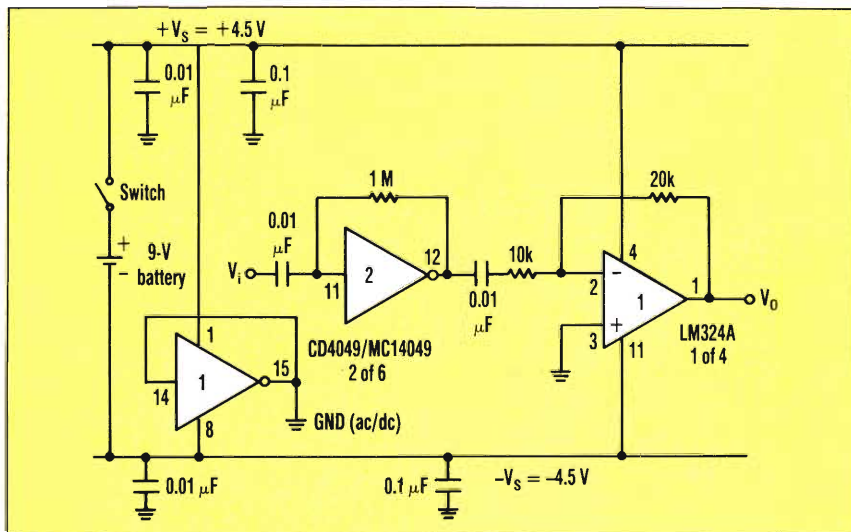
In communication and instrumentation design, particularly for battery-operated equipment, a simple, yet effective, amplifier component is occasionally needed. Such a component must exhibit good gain from base band through low IF frequencies with one inverting input. This component can be realized with a CD4049/MC14049 hex inverter buffer chip, a single-packaged CMOS SSI component. When an inverter is biased with one resistor from its input to output in the range of 100 k Ω to 10 M Ω and is capacitor coupled, it exhibits amplifier characteristics (see the table).

Furthermore, when a split power-supply bus is needed and only one battery is used, the inverter can be configured to supply a pseudo dc ground of relatively low impedance, coincident with the ac ground (see the figure). Depending on the magnitude of the dc ground return currents, anywhere from one inverter to several in parallel may suffice. Also, the supply buses must be capacitor bypassed.

INVERTER CHARACTERISTICS

	V supply	
	9V	13.6V
A_v	30 V/V	40 V/V
$f(-3dB)$	2.5 MHz	3.5 MHz nom.
I_{oh}	-1.25 mA	-3.0 mA min.
I_{ol}	8.0 mA	20.0 mA min.

The configured input-to-output-shortened inverter now acts as a voltage regulator that sinks and sources current. In this configuration, the inverter is forced to operate at the midpoint of its transfer characteristic. This divides the battery potential into two equal parts as referenced to the defined dc ground by virtue of its internal gain and physical structure. Op amps like the LM324A can be powered from one battery while referenced to the dc ground generated by the inverter. This novel technique surpasses the use of discrete resistors for battery potential dividing. It can be employed in other applications where individual component savings and improved design performance are needed. \square



TWO NOVEL USES for CMOS inverters appear in this circuit. Inverter 1 generates a pseudo dc ground for a split power-supply bus. Inverter 2 acts as a simple inverting amp.

CIRCLE
523 CHOPPER FETs
IMPROVE AMP

JIM WILLIAMS

Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035; (408) 954-8400.

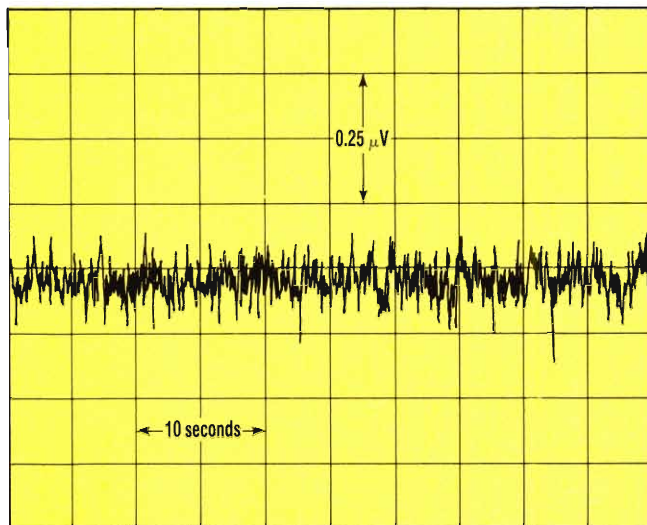
Combining the low drift of a chopper-stabilized amplifier with a pair of low-noise FETs results in an amplifier with 0.05- $\mu\text{V}/^\circ\text{C}$ drift, offset within 5 μV , 50-pA bias current, and 200-nV noise in a 0.1- to 10-Hz bandwidth. The noise performance is especially noteworthy because it's almost eight times better than monolithic chopper-stabilized amplifiers.

The FET pair (Q_1) differentially feeds A_2 to form a simple low-noise op amp (Fig. 1). Feedback, supplied by R_1 and R_2 , sets the closed-loop gain (1000 in this case). Although Q_1 has very low noise characteristics, its 15-mV offset and 25- $\mu\text{V}/^\circ\text{C}$ drift are poor. A_1 , a chopper-stabilized amplifier, corrects these deficiencies by measuring the difference between the amplifier's inputs and adjusting Q_{1A} 's channel current to minimize the difference. Q_1 's skewed drain values ensure that A_1 will be able to capture the offset. A_1 sup-

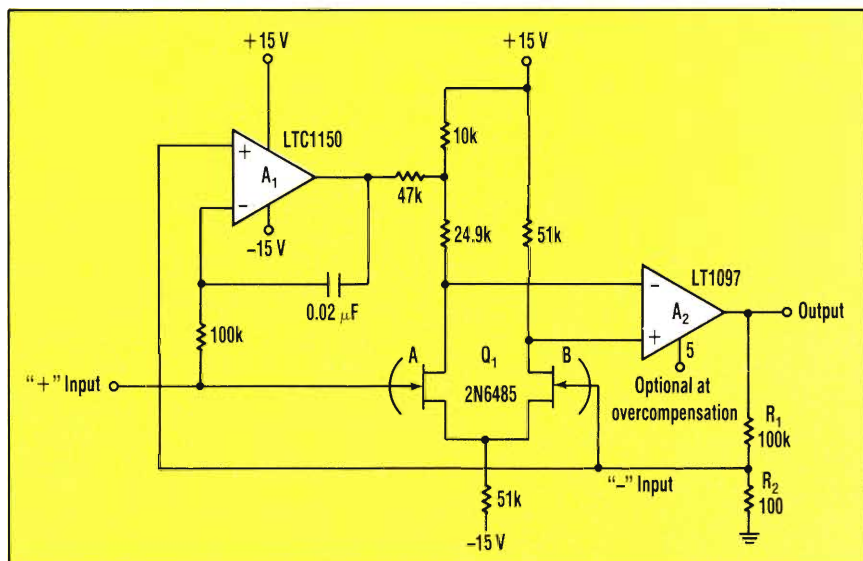
plies whatever current is required into Q_{1A} 's channel to force the offset within 5 μV . Also, A_1 's low bias current doesn't appreciably add to the overall 50-pA amplifier bias current. As

shown, the amplifier is set up for a noninverting gain of 1000, although inverting operation and other gains are possible.

The circuit's noise performance—measured in a 0.1-to-10-Hz bandwidth—is almost an order of magnitude better than any monolithic chopper-stabilized amplifier (Fig. 2). Yet it still retains low offset and drift. A_2 's optional overcompensation can be used to optimize damping when low closed-loop gains are used. □



2. PLOTTED IN A 0.1-to-10 Hz bandwidth, the circuit's noise is eight times better than monolithic chopper-stabilized amplifiers.

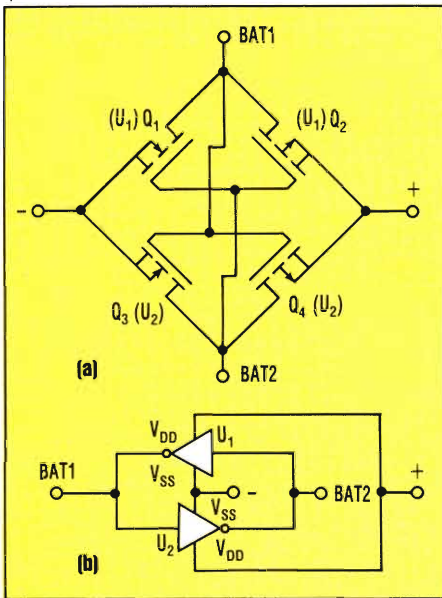


1. THE CHOPPER-STABILIZED FET PAIR combines the best of both worlds. Q_1 exhibits extremely low noise, and its offset and drift are reduced with A_1 , a chopper-stabilized amplifier.

CIRCLE 521 ACTIVE BRIDGE USES CMOS GATES

DAVE CUTHBERT

Tektronix Inc., P.O. Box 500 W3/100, Beaverton, OR 97077; (503) 690-7036.

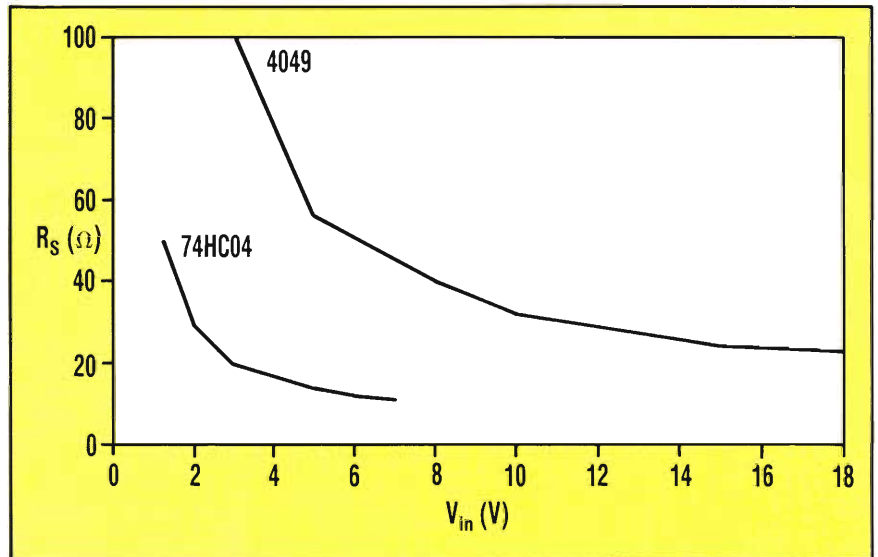


This bridge circuit, using two CMOS hex inverter chips, ensures that a battery supplies the correct polarity, regardless of how the terminals are connected (Fig. 1a). All six gates are paralleled in inverter U_1 to form one

low-impedance inverter. Inverter U_2 is connected in the same configuration.

A simplified schematic shows that when BAT1 is positive and BAT2 is negative, FETs Q_2 and Q_3 are on (Fig. 1b). When BAT1 is negative and BAT2 is positive, transistors Q_1 and Q_4 are on.

Inputs of 1.5 to 7 V can be used if the circuit is built with 74HC04 chips. Using 4049 chips boosts the allowable voltage ranging up to 3 to 18 V (Fig. 2). The bridge can also be employed as an active rectifier for square-wave signals. □



1. TWO CMOS HEX inverter chips are configured to form an active bridge, thus supplying the correct polarity to the circuit (a). In a simplified schematic, it can be seen that when BAT1 is positive and BAT2 is negative, transistors Q_2 and Q_3 are on; when BAT1 is negative and BAT2 is positive, transistors Q_1 and Q_4 are on (b).

2. TWO DIFFERENT CHIPS CAN BE USED FOR DIFFERENT voltage ranges, 74HC04s or 4049s. The bridge resistance is graphed against the varying supply voltages.

CIRCLE 522 GENERATE PARITY FOR 6805 CHIP

NOOR SINGH KHALSA

EG&G Inc., P.O. Box 809, MS E-1, Los Alamos, NM 87544; (505) 667-0200.

The full-duplex, asynchronous serial communication port of the Motorola 68HC05 family of low-cost, single-chip static microcontrollers contains an optional ninth bit that can be employed as a parity bit. However, the microcontroller doesn't contain a parity flag for the accumulator. One possible way to generate parity for

the microcontroller is to shift and count carries. Another method, one that's faster and less time-variant, is a software implementation of the old 9-bit odd/even TTL parity-generator-checker IC, the 74180 (see the figure). Using this procedure, alternate

PARITY:	STA	TEMP1	; Save a copy of the data byte in local RAM
	LSRA		; Shift Accumulator once
	EOR	TEMP1	; Exclusive OR even bits with odd bits
	STA	TEMP1	; Save a copy of the intermediate result
	LSRA		; Shift Accumulator twice
	LSRA		
	EOR	TEMP1	; Exclusive OR alternate intermediate bits
	AND	#\$11	; Mask off all but bit 4 (parity of upper
			; nybble) & bit 0 (parity of lower nybble)
	BEQ	P2	; If both bits are zero, parity is zero. Z flag = 1
	EOR	#\$11	; XOR with 11H. If both bits are 1, parity is zero
P2:	RTS		; Otherwise Acc has a value of 01H or 10H, Z = 0

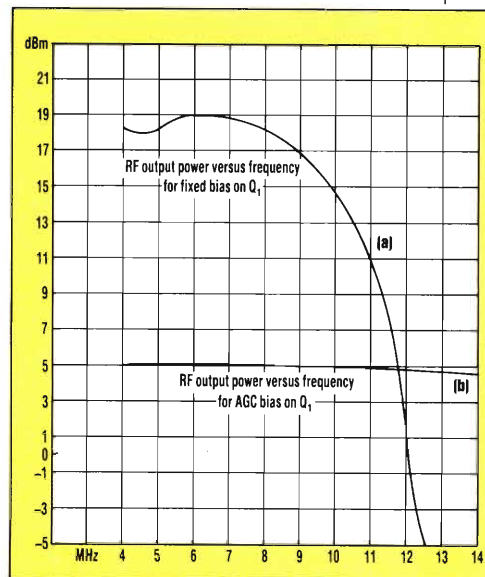
CIRCLE 521 AGC GIVES TOP TUNING RANGE

JOHN DUNN

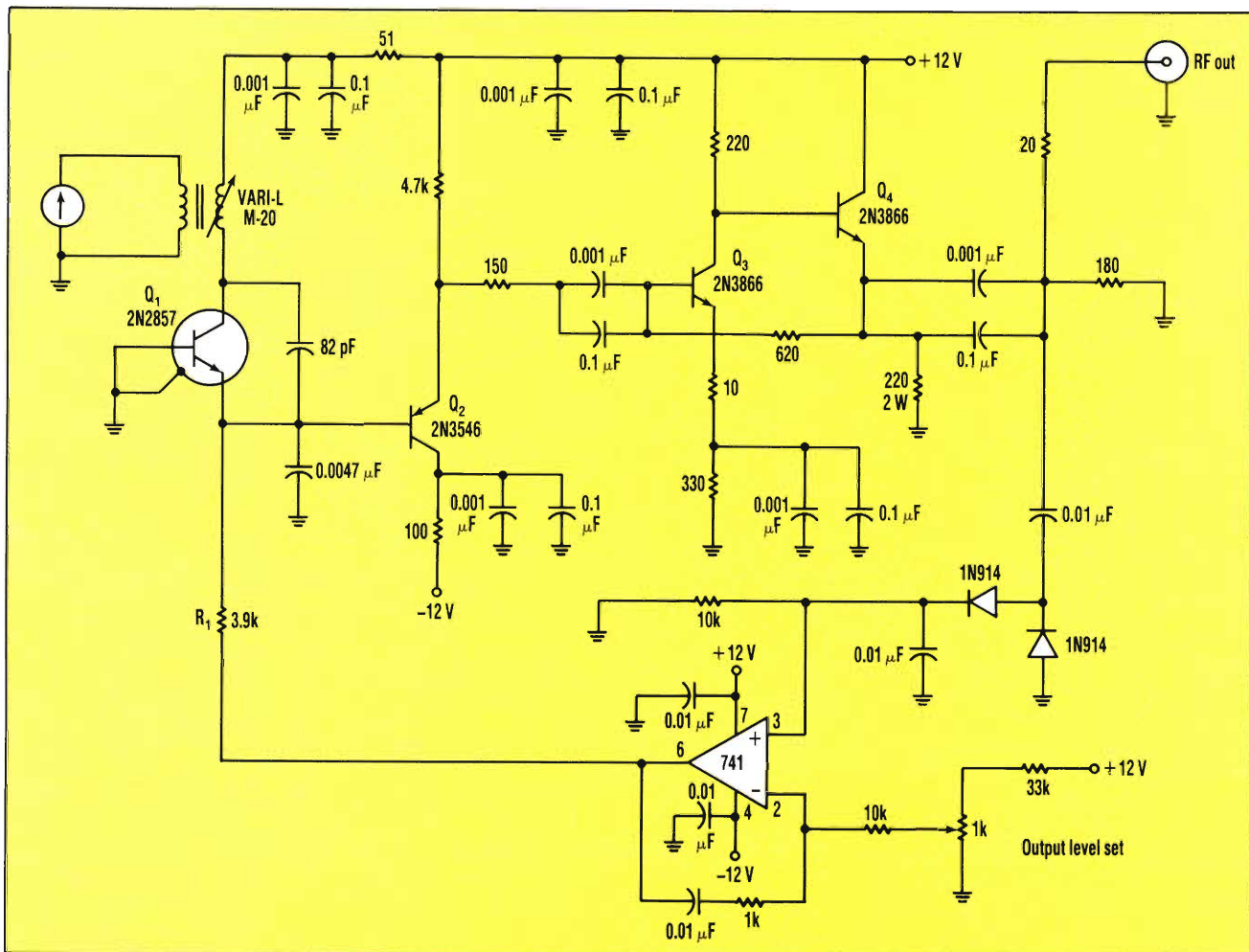
181 Marion Ave., Merrick, NY 11566.

This variable frequency oscillator can be tuned from 4 to 14 MHz using a current-controlled variable inductor (Fig. 1). The RF output power delivered to the load is stabilized by an automatic-gain-control (AGC) loop. Without the AGC loop, the full tuning range couldn't have been achieved. This is illustrated in the power versus frequency curves, which show the dramatic effect the AGC loop has in leveling the output power. (Fig. 2).

Without AGC, the changing LC ratio of the oscillator tank circuit causes the RF amplitude to vary so much versus frequency that the full frequency range can't be achieved. However, with AGC feedback applied to transistor Q₁, the transconductance of the transistor is adjusted automatically to the value that's required to produce the desired output level. As a result, the full tuning range that's specified for the variable inductor can be properly exploited. □



2. WITHOUT THE AGC loop, the oscillator's output varies with frequency (a). The output is stable with the loop (b).



1. BY USING A current-controlled variable inductor, this variable frequency oscillator can be tuned from 4 to 14 MHz. The wide tuning range is achieved with an automatic-gain-control loop.

CIRCLE 521 LOW-COST ISO AMP HAS HIGH PRECISION

JAMES WONG

Analog Devices Inc., 1500 Space Park Dr., Santa Clara, CA 95052; (408) 727-9222.

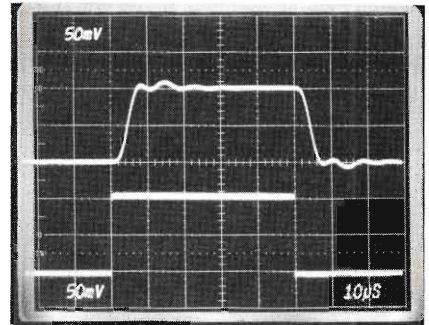
An isolation amplifier that can work across a 5000-V barrier with a maximum dc gain error of only 0.1% can be built using a bifurcated linear optocoupler at a parts cost of about \$7 or \$8 (Fig. 1). The amplifier is at least as good as most commercial units, which cost up to \$100.

Key to the amplifier's operation is the optocoupler, which contains one LED and two nominally identical photodiodes. One of the photodiodes is on the same side of the 5000-V isolation barrier as the LED. It's used in a feedback loop to ensure a linear relationship between the amplifier's input voltage, V_{in} , and the photocurrents in the two photodiodes, independent of temperature variations and long-term drift of the LED's output.

The amount of light received by the second LED is linearly propor-

tional to the amount received by the first one; hence its photocurrent is also proportional to V_{in} . That photocurrent is converted back into a voltage by the output op amp. The isolation amplifier requires two separate, isolated power supplies: one for the input circuitry, and one for the output.

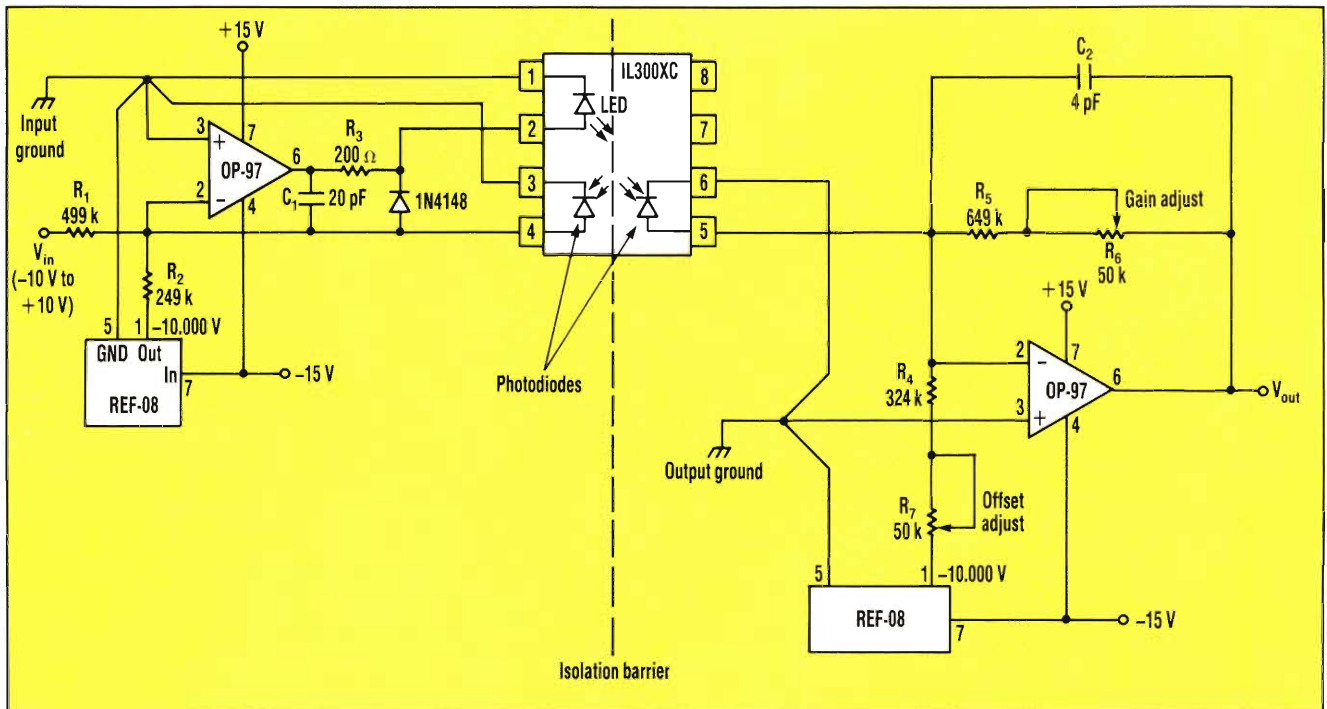
Because current can flow through the optocoupler's LED in only one direction, the input op amp is biased by a -10.000-V reference supply, through R_2 . Consequently, the amplifier can handle bipolar input signals in the range of ± 10 -V. It exhibits a linearity of better than 0.05% over that range. To minimize the errors generated by the isolation amplifier's relatively high circuit resistances, the op amps were chosen for their low input bias currents and low temperature-drift characteristics. Thus, the overall amp can maintain



2. THIS SCOPE PHOTO of the amplifier's small-signal pulse response (input on lower trace, output on upper trace) demonstrates the unit's bandwidth characteristics. The amplifier's response extends out to 85 kHz.

its dc gain at 1.000 ± 0.001 from 0° to 70° C.

The amplifier has two simple adjustments—offset and gain. The offset pot (R_7) is adjusted for zero output with 0 V applied to the input. The gain pot (R_6) is trimmed for -10.000 V out, with -10.000 V in. Repeat the sequence until no further adjustment is needed. The amplifier has a respectable 3-dB bandwidth of 85 kHz (Fig. 2). □



1. THE "EXTRA" photodiode on the input side of the optocoupler provides feedback, which gives the isolation amplifier its excellent (0.05%) linearity. Note that the amplifier requires independent power supplies for its isolated input and output circuits.

CIRCUIT PASSES ONLY HIGH-SPEED DATA

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Serial data communications lines sometimes carry a mixture of narrowband and wideband information (Fig. 1, top line). If it's desirable to use the wideband signal and ignore the lower-speed component—to extract a clock, for example—a simple one-shot circuit can do the job (Fig. 2).

The circuit is essentially a timed gate that opens when the high-frequency signal is present, and stays closed at all other times. The gate is controlled by a pair of one-shots whose on-time (t_{os}) is chosen to be greater than the period of the high-frequency signal but shorter than half the period of the low-frequency one.

The gate passes the input signal only while both one-shots are on—while both of their outputs are low. At all other times, the output of the OR gate simply stays high. The one-shots are retriggerable so their outputs stay low and the gate stays open continuously as long as the high-frequency

input is present.

Gate IC₂ can be realized in a number of ways. One of the simplest is as a combination of 74LS32 quad two-input OR gates.

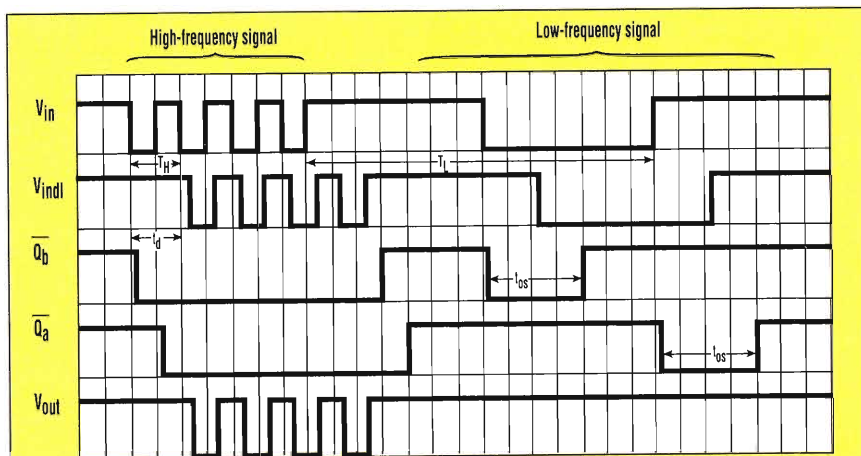
If the high-frequency signal has a frequency f_H (with a corresponding

period T_H) and the low-frequency signal has a frequency f_L (with a corresponding period T_L), then the condition for passing the higher frequency and suppressing the lower one is:

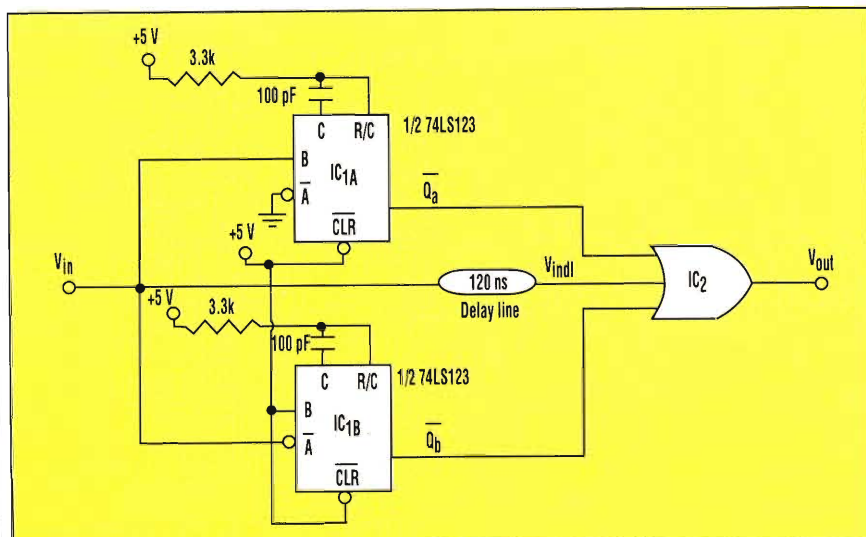
$$T_H < t_{os} < T_L/2.$$

Frequencies between f_L and f_H are not permitted.

The delay line introduces a small fixed delay, t_d , into the main signal path to give the one-shots time to change state. Doing so ensures that the one-shot propagation delay time, t_p , does not cause the first bit in the



1. SERIAL BIT STREAMS often contain a mixture of high- and low-frequency components (V_{in}). A gate controlled by signals Q_b and Q_a can suppress the low-frequency signal, leaving just the high-speed data out.



2. TWO ONE-SHOTS form the heart of a simple circuit for extracting fast-switching signals from a serial bit stream. When built with the component values shown, the circuit will pass all frequencies above 8 MHz and block those below about 2 MHz.

data stream to be lost. The condition for saving the first bit is:

$$(T_{os} - T_H/2) > t_d > (T_H/2 + t_p).$$

Because component tolerances and variations in the frequency of the input signal can affect circuit operation by causing a frequency to fall into the forbidden region, it is best to allow generous margins when configuring a system. The circuit of Figure 2, for example, is designed for a maximum T_H value of 125 ns, a minimum T_L value of 500 ns, a t_{os} of 200 ns, and a t_d of 120 ns. It is thus rated to pass all frequencies above 8 MHz and to block all frequencies below about 2 MHz with comfortable margins. For the numbers in the example, the condition on T_H and T_L (first inequality) becomes: 125 ns < 200 ns < 250 ns. □

CIRCLE 521 VARY CAPACITANCE TO POSITIVE OR NEGATIVE

JOHN DUNN

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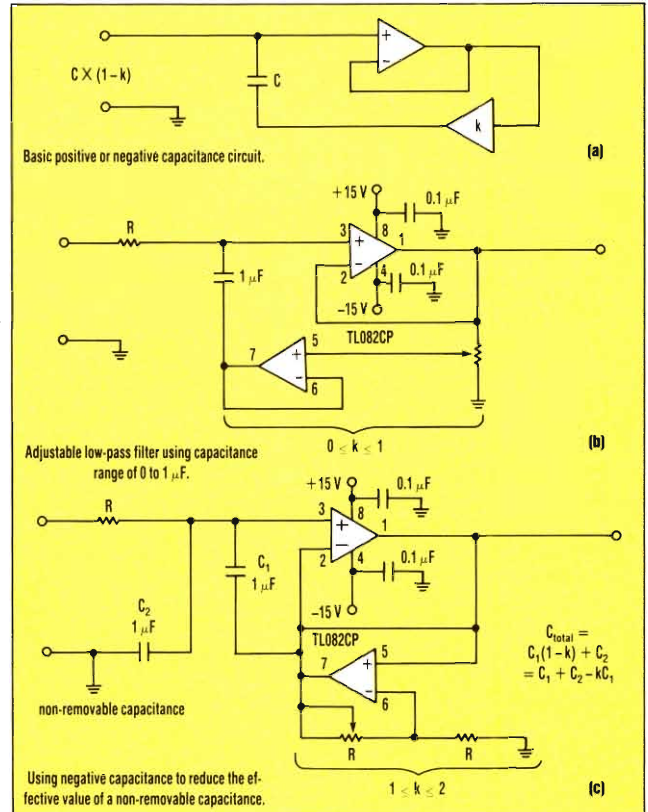
There are at least two reasons to use this basic circuit whose equivalent capacitance can be made positive or negative (Fig. 1a). First, variable capacitances can be obtained in value ranges not readily available in physical structures. Second, an existing shunt capacitance can be made adjustable either above or below its existing value.

The circuit's equivalent capacitance is $C \times (1 - k)$, where k is adjustable. The effective capacitance is varied by adjusting k . Consider a simple low-pass filter (Fig. 1b). If $C = 1.0 \mu\text{F}$, adjusting k from 1 to 0 gives a 0- to $1.0\text{-}\mu\text{F}$ variable capacitance, effectively varying the filter's cutoff frequency. When k is greater than one, a negative capacitance is obtained. Thus, if a circuit has a large, unwanted, and nonremovable capacitance to ground, that capacitance could be reduced by paralleling it with an adjustable negative capacitance (Fig. 1c). As before, if $C_1 = 1.0$

1. THE equivalent capacitance of this circuit can be made positive or negative by varying k (a). By setting k from 1 to 0, a variable capacitance of 0 to $1 \mu\text{F}$ is obtained. This varies the cutoff frequency of a simple low-pass filter (b). Non-removable capacitance can be reduced by paralleling it with an adjustable negative capacitance (c).

μF , adjusting k from 1 to 2 gives a 0 to $-1.0\text{-}\mu\text{F}$ capacitance.

The absolute value of the negative capacitance shouldn't be greater than the positive value being paralleled or the circuit will oscillate. □



CIRCLE 522 DRIVERS FOR STEPPER MOTORS GET SIMPLER

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This design for a stepper-motor driver was inspired by two previously published circuit designs (ELECTRONIC DESIGN, May 10, 1990, p. 103, and May 23, 1991, p. 120). Simpler than its predecessors, it uses only two common integrated circuits, yet contains its own clock generator.

The heart of the driver is a 74HC194 4-bit bidirectional shift register, IC₂, which assigns the motor steps (see the schematic diagram). The register shifts either left or

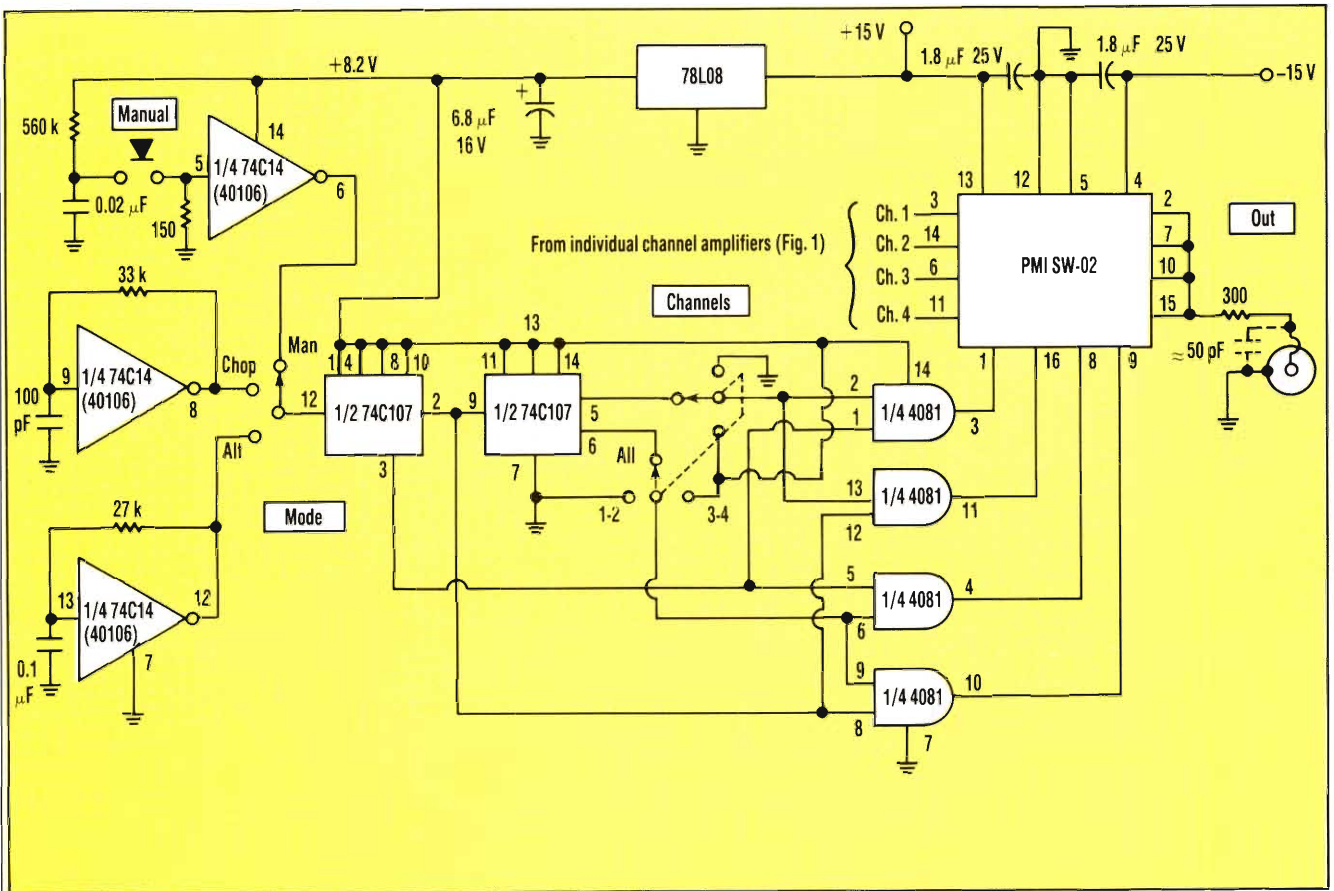
right depending on its S_0 and S_1 inputs. When $S_0 = 0$ and $S_1 = 1$, it is a left shift register. If the signals are reversed, so is the shifting direction. The shift left (S_L) and shift right (S_R) inputs are connected to Q_A and Q_D , respectively.

Thus, if a logic ONE is somehow stored in the register, it can be shifted right or left by the clock. At any time there is one and only one active phase, and its shifting direction determines the motor direction.

The trick is to insert the logic ONE

into the shift register. That is accomplished by the Clear signal, with capacitor C_3 and resistor R_4 , which form a differentiator. When the Clear signal goes from high to low (see the timing diagram), the differentiator produces a narrow negative pulse at Point A to reset IC₂. As the Clear signal remains low, points B and C are kept high, which sets IC₂ into Load mode. Then the low-to-high jump of the Clear signal acts as an extra clock pulse, loading a ONE into input A of IC₂. Because inputs B, C, and D are tied to ground and thus constrained to be ZEROs, the required single ONE is thus loaded.

With the Clear signal high, the clock generator formed by NAND gate IC_{1A}, resistor R_1 , and capacitor C_1 begins to work. The motor speed is controlled by the clock frequency, hence the desired speed can be ob-



2. THE QUAD ANALOG switch at the heart of this multiplexer accepts the signals from the four amplifiers of Fig. 1 and sends them to the oscilloscope. The approximately 50 pF of capacitive loading at the multiplexer's output represents the scope's input capacitance plus that of the connecting cable. The Channel and Mode switches are of the non-shorting type.

individual channel amplifiers shown in Fig. 1. They can be made with either LF351 (low noise) or LM318 (high speed) op amps. The values of C_1 and C_2 appropriate for each op amp are shown in the table in the lower left-hand corner of Fig. 1.

The outputs of the individual chan-

nel amplifiers feed into a multiplexing section based on a PMI SW-02 quad JFET analog switch, which in turn feeds into the scope (Fig. 2). The multiplexer has a 170-kHz Chop mode for sweep speeds of 0.5 ms/div and below; an Alternate mode for rates of 0.2 ms/div and above; and a

Manual stepper mode. The stepper mode cycles through the channels, displaying a different single trace each time the Man button is pushed. The Channels switch allows the display of all four channels simultaneously, channels 1 and 2 only, or channels 3 and 4 only. □

CIRCLE 522 AC AMPLIFIER PASSES LOW FREQUENCIES

JOHN DUNN

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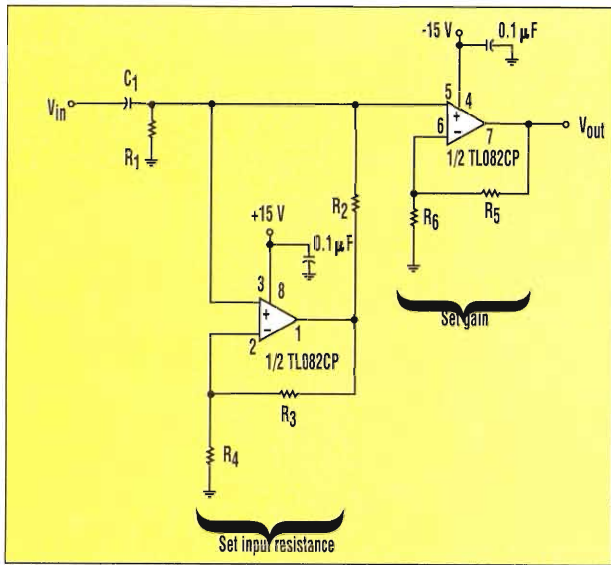
Ac-coupled amplifiers frequently have low-frequency cutoff points in the vicinity of 20 Hz—at the low end of the audio spectrum. For applications that require passing much lower frequencies while still blocking dc,

the design of such amplifiers can get difficult, requiring either an extremely large capacitor, compromises in input impedance and gain, or quite possibly, both.

By basing the amplifier on a negative-resistance converter instead of

on the more common technique of input bootstrapping, it is possible to build a device with an extremely low cutoff frequency, a modest-sized capacitor, and independently adjustable gain and input resistance (see the figure).

The first stage of the two-stage amplifier is a negative-resistance converter, which sets the amplifier's input resistance. Together with capacitor C_1 , that resistance establishes the low-frequency cutoff point. The independent second stage sets the amplifier's gain.



INDE-
pendently
adjustable gain and
input resistance are
two features of this
very low cutoff ac-
coupled amplifier.
Because the
negative resistance
converter input
stage makes
possible extremely
high input
resistances, the
input capacitor can
be of modest size
and still pass
frequencies below
one hertz.

The formulas for input resistance, cutoff frequency, and gain are as follows:

$$R_{in} = R_1 R_2 R_4 / (R_2 R_4 - R_1 R_3)$$

$$f_{co} = 1 / (2\pi R_{in} C_1)$$

and

$$G = (R_5 + R_6) / R_6$$

Referring to the diagram, if $R_1 = R_2 = R_4 = 100 \text{ k}\Omega$ and $R_3 = 97.6 \text{ k}\Omega$, then the input resistance is raised from the 100-k Ω value of R_1 to approximately 4 M Ω . With that resistance, a moderate sized input capacitor, C_1 , of 0.1 μF will give a cutoff frequency of approximately 0.4 Hz. The upper cutoff frequency of the amplifier is determined mostly by the op amp characteristics, in this case a dual TL082CP. □

CIRCLE 523 GET +5V/100 MA FROM FOUR CELLS

MITCHELL LEE

Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035; (408) 432-1900.

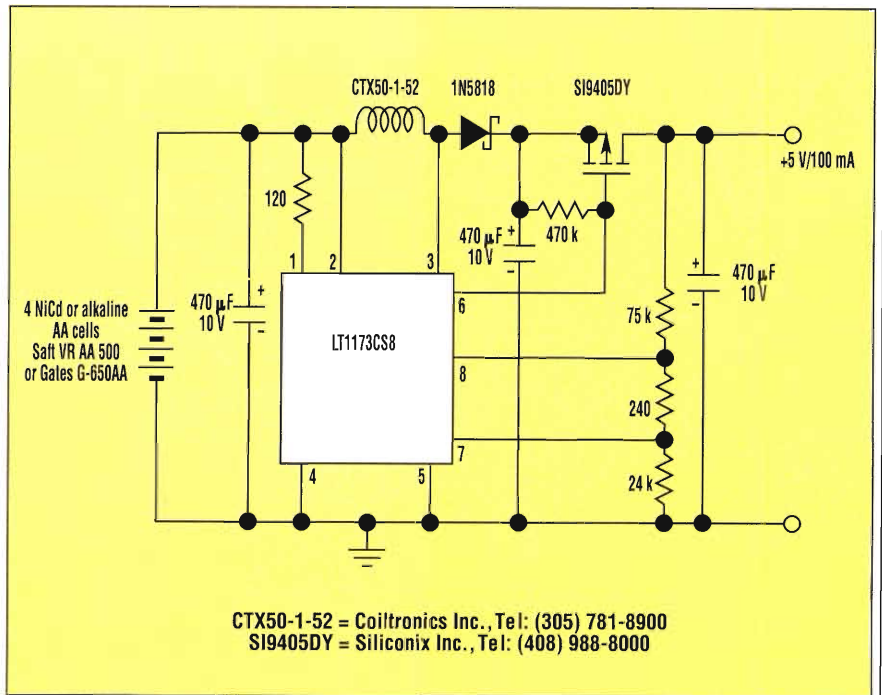
In many instances, a four-cell battery is the popular choice for portable instruments. But this poses a special problem for instruments with 5-V circuits—the battery's terminal voltage isn't well behaved. For example, a battery of four, fresh alkaline cells develops about 6.5 V, but at end-of-life the voltage falls to 3.6 V under load.

NiCd cells have only a slightly narrower range—about 4 V to 6 V. A fly-back topology dc-dc converter can handle the job, but requires a tricky transformer design.

A unique solution to the problem is based on a dual-mode conversion circuit (see the figure). Producing a 5-V, 100-mA output from a four-cell input, the converter only requires a simple two-terminal inductor. At input voltages below 5.5 V, the circuit operates as a burp-mode boost converter, with the MOSFET held in the On state. At higher input voltages, the boost converter shuts down and the MOSFET acts as a series pass element in a very-low-dropout regula-

tor. The error amplifier is contained in the LT1173CS8 micropower dc-dc converter.

Because it operates with inputs ranging from 3.6 to 7 V, the converter allows direct interchanging of alkaline and NiCd cells. It also permits in situ charging of NiCd cells. □



CTX50-1-52 = Coiltronics Inc., Tel: (305) 781-8900
SI9405DY = Siliconix Inc., Tel: (408) 988-8000

USING A SIMPLE two-terminal inductor, this dual-mode, dc-dc converter operates with battery terminal voltages ranging from 3.6 to 7 V. When the battery voltage falls below 5.5 V, the circuit operates as a burp-mode boost converter. At higher voltages, it functions as a very-low-dropout regulator.

CIRCLE 521 FEEDBACK LINEARIZES CURRENT SOURCE

JERALD GRAEME

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Many adjustable dc current sources typically exhibit nonlinear control characteristics—most often an inverse relationship between pot rotation and current. That nonlinearity, which is most pronounced at high current levels, means that the control tends to be hypersensitive at one end of its adjustment range and unresponsive at the other. By employing bootstrap feedback (see the figure), it's possible to provide an inherently linear control that works equally well at all current levels.

Reduced to its essentials, the circuit consists of a voltage reference (IC₁), which drives a load (Z_L) through a sensing resistor (R_S). Amplifier feedback controls the voltage across R_S to set the current.

Unlike conventional implementations that adjust the current by varying R_S, the bootstrap circuit varies the voltage directly by controlling the bootstrap gain. That produces direct, rather than inverse, proportionality between the control setting and the output current.

Potentiometer R_V varies the bootstrap gain to control the fraction of reference voltage V_R that appears across R_S. Op-amp feedback forces that voltage, V_S, to equal the voltage

across the xR_V portion of R_V.

Because the voltage reference is in parallel with the control pot, the voltage across R_V is constrained to be V_R, and the voltage fraction across xR_V is simply xV_R. The voltage across the sensing resistor is the same. Hence, the output current is given by: I_O = xV_R/R_S. For the components shown in the diagram, I_O can be varied from 0 to 1.25 A.

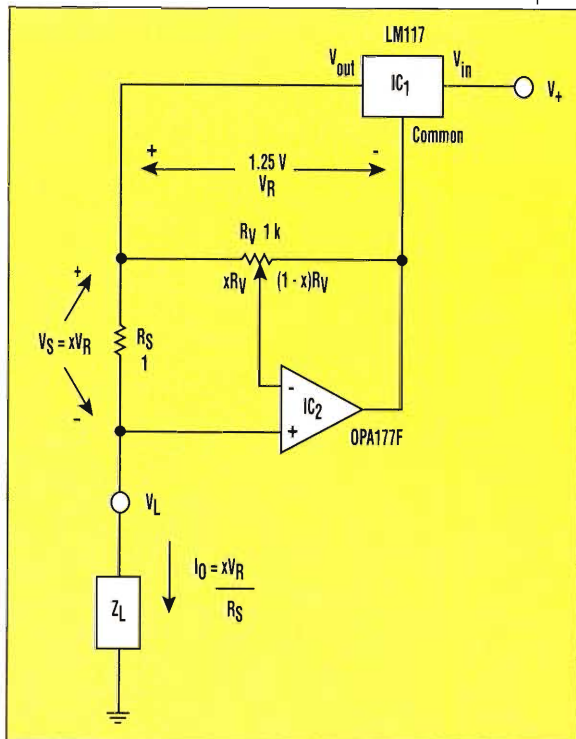
In addition to linearizing the current control, this approach keeps the control potentiometer out of the main current path. Because the pot needn't carry the full output current, it can have a high value, making its end resistance negligible. That eliminates an extra source of nonlinearity.

With nonlinearity removed, component errors set the limits on circuit performance. The LM117 regulator drifts 0.01% per °C and R_S may drift 0.015% per °C. Thus, even assuming that all errors have been trimmed out at nominal temperature, a ±5°C environment limits trim accuracy to around 0.125%.

Error also results from a circuit output resistance of:

$$R_O = R_S / (xL_R + 1 / PSRR)$$

where L_R is the line regulation of the regulator and PSRR is the power-supply rejection ratio of the amplifier. For the components shown, and x = 1, R_O = 8 kΩ. A 10-V change in load voltage produces a 0.1% change in output current. □



LINEAR CURRENT CONTROL results from bootstrap feedback, which redefines the control characteristic. This circuit has a current range of 0 to 1.25 A, an output resistance of 8 kΩ, and a maximum drift of 0.025% per °C.

CIRCLE 522 TURN SCOPE INTO CURVE TRACER

LESTER R. ORENSE

Allegro Microsystems Philippines, Inc., Sampaguita St., Marimar Village, Parañaque, Metro Manila, Philippines 1700; Tel.: (632) 828-90-26;

Fax: (632) 828-40-45.

An inexpensive yet effective way to evaluate semiconductor component quality is to display the device's I-V characteristics on an oscilloscope. Sharp, clear transitions indicate

“healthy” junctions (Fig. 1). Soft, gradual ones imply leakage or possibly even shorts.

All that's needed to set up an appropriate I-V display are a pair of dual op amps and a handful of pas-

sive components (Fig. 2). Op amp A_{1A} generates a 300-Hz sine wave with a peak-to-peak amplitude of 20 V. That sinusoid is buffered by op amp A_{1B} to drive the device under test (DUT).

Op amp A_{2A} provides a return path for the current from the DUT and converts that current into a voltage. Finally, op amp A_{2B} inverts the voltage before feeding it to the scope for a correct I-V display.

The scope must, of course, be in its X-Y mode. A good initial gain setting is about 2 V/division.

In addition to individual compo-

CIRCLE
523 **DIGITAL PLL**
SUITS FPGAS

DENNIS McCARTY

Actel Corp., 955 East Arques Ave., Sunnyvale, CA 94086; (408) 736-1030.

In telecommunications applications, it's often desirable to generate a digital signal that's locked to an incoming signal and is some multiple of its frequency. A simple way to generate such a signal uses a pulse-steal phase-locked loop, or PLL (see the figure). The design contains an ordinary oscillator, but no voltage-controlled oscillator (VCO). And, except for the crystal, the entire design will operate in an FPGA.

Consider the frequency relationship at points A and B in the circuit:

$$OSC/(K \times M) = F_{in}/N = F_{comp}$$

where OSC = effective reference frequency and F_{comp} = comparison frequency.

The technique is based on selecting a reference oscillator frequency which is slightly higher than OSC. This frequency (OSC+) should be chosen so that:

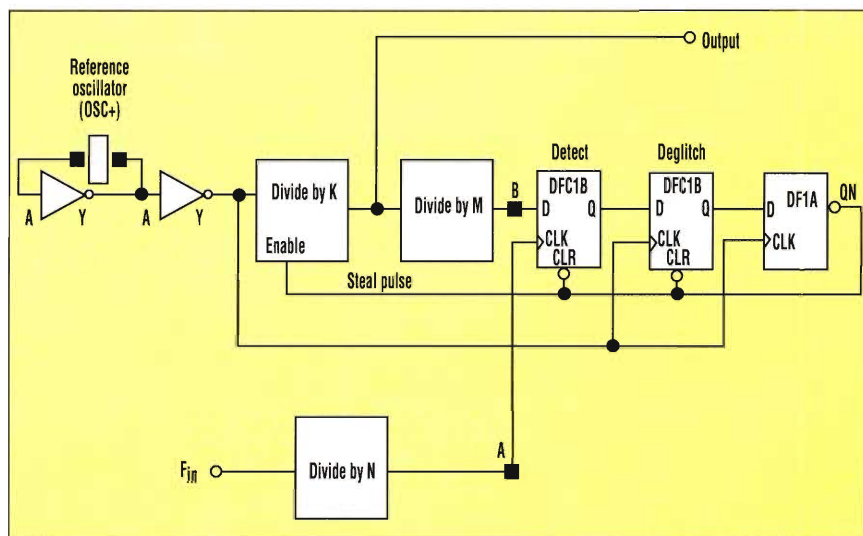
$$(1/F_{comp}) - (K \times M)/(OSC+) = 0.5(1/OSC)$$

The right side of this equation equals one-half the period of the reference oscillator.

The reference-oscillator frequency delta will cause point B (the detector flip-flop D input) to begin to precede point A (the detector flip-flop clock input) by half a period each comparison interval. When the edge of the D input advances sufficiently, the detector will clock true and begin a pulse train through the two deglitching flip-flops. The output of the second of these clears all three flip-flops and steals a pulse by disabling the divide-by-K output. Stealing the pulse puts point B behind point A until the reference-oscillator delta can move it ahead by one period—thereby repeating the cycle. Points A and B are always within one-half a cycle of each other.

To select the output signal's frequency, simply adjust the values of dividers K and M. The lock range of the loop is given by:

$$\text{Lock Range} = \pm(OSC+/OSC)/F_{in} \square$$

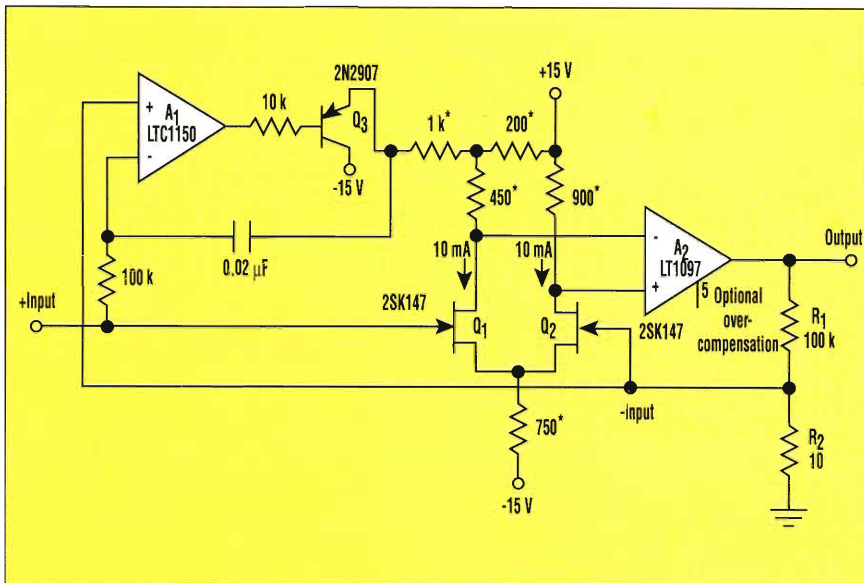


THIS DIGITAL PLL, which contains no VCO, relies on a pulse-stealing technique that always keeps points A and B within one-half cycle of each other. This action keeps the loop locked.

CIRCLE
**521 AMP MINIMIZES BOTH
 DRIFT AND NOISE**

JIM WILLIAMS

Linear Technology Corp., 1630 McCarthy Blvd.,
 Milpitas, CA 95035-7487; (408) 954-8400.



1. LOW-NOISE FETs Q_1 and Q_2 minimize the noise level of this chopper-stabilized amplifier. For best performance, the Toshiba 2SK147 FETs must be V_{gs} matched to within 10% and thermally mated. The resistors marked with an asterisk are 1% thin-film devices.

Usually, amplifier users must decide between the lesser of two evils: the low drift of a chopper-stabilized unit or the low noise of an unstabilized device. No more. By combining a pair of low-noise FETs with a chopper-stabilized amplifier, this circuit has just $0.05 \mu\text{V}/^\circ\text{C}$ of drift and less than 50 nV of noise in the band from 0.1 to 10 Hz (Fig. 1). Moreover, its offset is less than $5 \mu\text{V}$, and its bias current is less than 100 pA . Putting that performance in perspective, the noise is almost 35 times less than that of monolithic chopper-stabilized amplifiers. As shown, the amplifier is configured to provide a noninverting gain of 10,000; other gains and inverting operation are possible.

Key to the amplifier's performance are low-noise FETs Q_1 and Q_2 , which differentially feed amplifier A_2 to form a simple low-noise op amp. Feedback, via R_1 and R_2 , sets the closed-loop gain (to 10,000 in this

case) in the usual fashion.

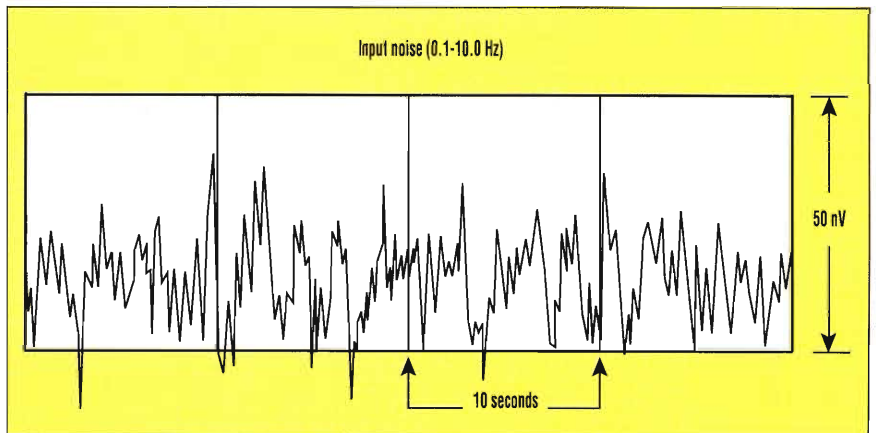
Although Q_1 and Q_2 have very low noise, their offset and drift are uncontrolled. Those deficiencies are corrected by amplifier A_1 , a chopper-stabilized device. A_1 does that by measuring the difference between the inputs to Q_1 and Q_2 and adjusting

Q_1 's channel via Q_3 to minimize that difference. Because there's no way to predict the offset's sign, the FET drain resistor values are purposely skewed enough to force the offset in the right direction—that is, to make its sign so that A_1 can capture it.

In building the amplifier, care must be taken to select the FETs so that their gate-source voltages (V_{gs}), which can vary over a 4:1 range, match within 10%. That will allow A_1 to capture the offset without introducing any significant noise.

Because Q_1 and Q_2 run with 10-mA channel currents, they will experience a significant temperature rise. To obtain the specified noise performance, it's necessary that they be thermally mated and shrouded. Otherwise, small air currents could create temperature differences sufficient to increase noise by an order of magnitude. The thermal shrouding should completely enclose both devices and extend all the way down to the circuit board. Properly built, the amplifier will exhibit input noise characteristics as good as those of the best bipolar amplifiers (Fig. 2).

The transient response of the amplifier is clean, with no overshoots or uncontrolled components. If A_2 is replaced with a faster device, such as an LT1055, the speed can be increased by an order of magnitude with similar damping. A_2 's optional overcompensation capability (capacitor to ground) can be used to optimize response for low closed-loop gains. □



2. AS QUIET AS the best bipolar amplifiers, this FET-input circuit generates less than 50 nV of peak-to-peak noise over the band from 0.1 Hz to 10.0 Hz .

CIRCLE 522 TESTER FINDS SHORTS ON LOADED BOARDS

ALEXANDER L. BELOUSOV

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By combining a germanium diode with a low-voltage (1.5-V) supply, this simple tester can detect shorts and opens in cables and printed-circuit boards—even in the presence of mounted silicon semiconductors (see the figure). With the component val-

ues shown, the tester has a threshold of about 10 Ω . That is, the tester indicates a short circuit when it detects less than 10 Ω , and an open circuit otherwise. Its zone of uncertainty is about 2 Ω . The open-circuit voltage at the probe tips is about 200 mV—low enough not to turn on any silicon

devices. If the probe tips are shorted together, the current that flows will be less than 8 mA.

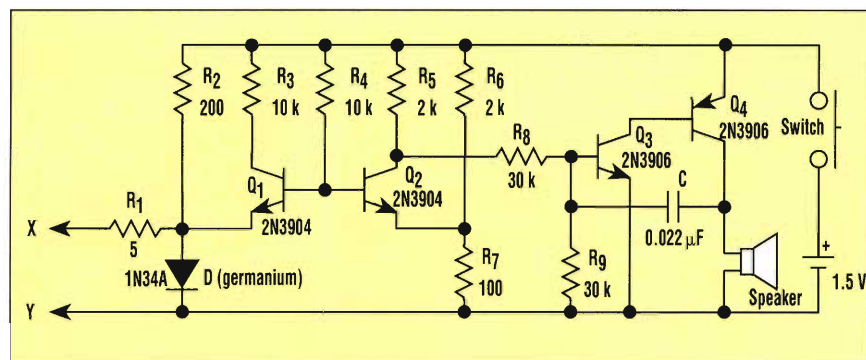
Transistors Q_1 and Q_2 , together with resistors R_1 through R_7 , make up the input balancing stage, which senses the resistance between points X and Y.

The input stage is essentially a bridge, consisting of R_1 , R_2 , R_6 , R_7 , and the resistance between X and Y.

Transistors Q_3 and Q_4 and their associated passive components form a buzzer, which sounds when the tester detects a short. The buzzer is controlled by the output from Q_2 . When the input resistance is high (more than about 10 Ω), Q_2 turns on, so its collector potential is close to ground, and the buzzer remains off.

When the input resistance is sufficiently low, Q_2 turns off, and the buzzer sounds. The frequency of the sound, which is about 1000 Hz, can be adjusted by varying the value of capacitor (C).

Although the tester calls for a 1.5-V supply, it will continue to function even when that voltage drops below 1.0 V. If desired, the input resistance threshold can be varied by changing resistor R_1 or R_2 . □



TO FIND SHORTS and opens on boards loaded with silicon components, this test circuit keeps its probe voltage below about 200 mV, low enough to ensure that silicon devices aren't turned on. The diode (D) is a germanium device.

CIRCLE 523 BOOTSTRAP CIRCUIT CUTS DISTORTION

WALT JUNG

Analog Devices Inc., 1 Technology Way, Norwood, MA 02062-9106; (617) 329-4700.

Standard-process junction-isolated FETs are popular items for IC op amps because they generally incur few dc errors and offer good ac performance. For example, total harmonic distortion (THD) can be as low as 0.001% (10 ppm) over the audio range.

But the fidelity of high-source-impedance, JFET op-amp circuits drops quickly as distortion rises with an increasing rate of change in the input signal. Fortunately, this distortion can be significantly reduced by using the op amp in a bootstrap circuit configuration.

The distortion problem arises from the nonlinearity of the capacitance at the JFET's two inputs. Typically, JFETs consist of a pair of differential p-channel FETs at the input and npn/pnp bipolar transistors for the remaining stages. The junction isolation is provided by isolation "wells" for the differential FET pair. These wells create a parasitic substrate capacitance of about 3 to 5 pF at the inputs.

The parasitic capacitance is nonlinear with the applied common-mode voltage, so it varies instantaneously with an ac input. When such an op

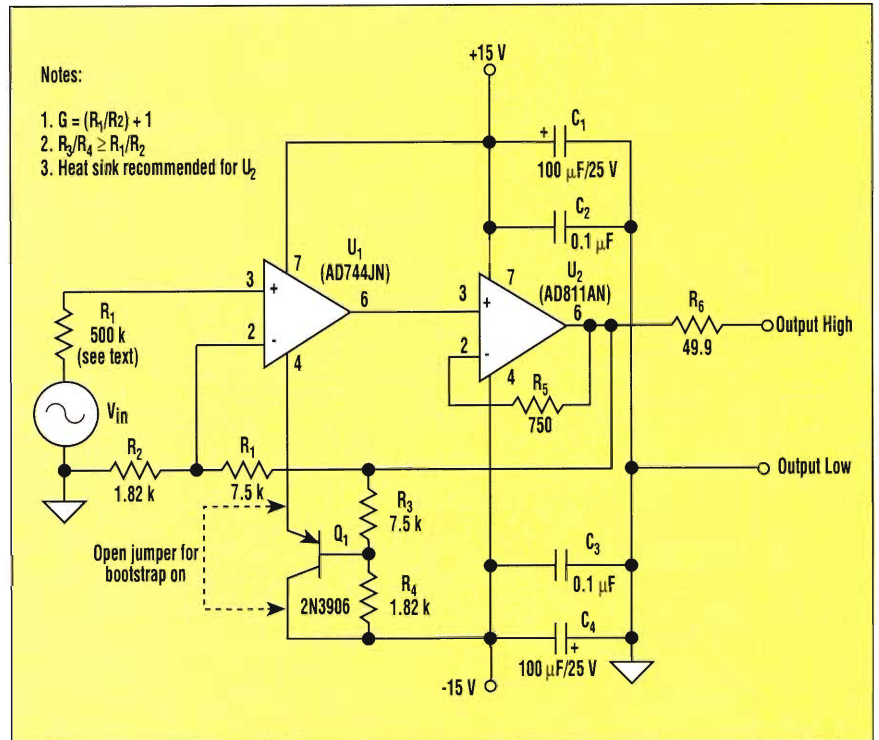
amp acts as a follower with high source impedance, it can generate excessive THD, which is seen as a 6-dB/octave rise in second-harmonic distortion with a fixed-level frequency sweep.

Bootstrapping reduces the effects of the capacitance. The bootstrap circuit is a second feedback divider referred to the negative supply that feeds back a signal to the V- pin, pin 4 (Fig. 1). When done properly, bootstrapping can cut capacitance-related distortion to below the residual noise level.

In the example circuit, U_1 , an AD744, is loaded only by the high-impedance input (the positive input) of U_2 , so U_1 provides virtually zero drive current.

This arrangement enhances the overall load-dependent linearity as well as the bootstrapping.

Unity-gain follower stage U_2 , an



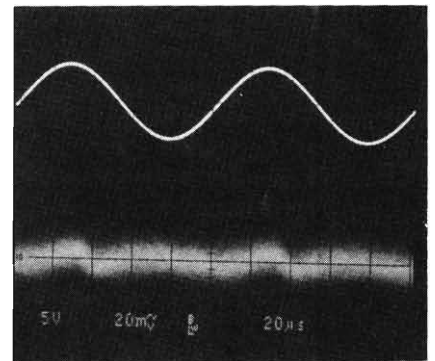
1. A SECOND FEEDBACK DIVIDER in a JFET op-amp circuit (R_3 and R_4) bootstraps U_1 's substrate. As a result, the distortion caused by nonlinear capacitance is reduced.

AD811AN, primarily supplies a 100-mA output drive and good linearity into 600- Ω (or lower) loads.

The circuit's overall voltage gain, G , is set by R_1 and R_2 , just as in a conventional noninverting amplifier. For the bootstrap divider, the ratio of R_3/R_4 must be the same or higher than R_1/R_2 . The values in the example deliver a gain of 5.12 (very low gains aren't recommended because they reduce dynamic range).

The bootstrap drives U_1 's substrate with a signal equal to that at the positive input. As a result, ac voltage is reduced across the nonlinear capacitance and there's less distortion. The bootstrapping will work without U_2 , but the distortion reduction won't be as great and it will vary with U_1 's loading.

In tests with ± 15 -V supplies and a 500-k Ω source, the THD of a non-bootstrapped circuit varied from about 0.01% at 1 kHz to 0.2% at 20 kHz. At 10 kHz and with a 3-V rms output from U_2 , THD was 0.1%. But with the bootstrap, the distortion at 10 kHz dropped by an order of magnitude, essentially disappearing into the residual noise (*Fig. 2*).



2. THE DISTORTION in a bootstrapped JFET op-amp circuit was cut by an order of magnitude, essentially fading into the residual noise (lower trace). The distortion analyzer was set to a full-scale range of 0.03%

The principles behind this distortion mechanism apply to virtually all JFET input op amps, regardless of source. Junction-isolated bipolar op amps can also exhibit the phenomenon and thus may benefit from bootstrapping.

But unlike JFET amps, bipolar types aren't as likely to be used with high source impedances, where this distortion is a problem. \square

CIRCLE
522 ADJUST TEMPCO
IN SIZE AND SIGN

MICHAEL A. WYATT

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Zeroing out temperature variations on a production line is a challenging task when the device to be compensated has a temperature coefficient that varies in both magnitude and sign from unit to unit.

This simple circuit can meet the challenge (see the figure). It's inexpensive and delivers an output voltage with a tempco that can be adjusted from -10 to +10 mV/°C for the values shown in the diagram.

The heart of the compensator is the Analog Devices AD590 temperature transducer, which may be located remotely if desired. The device produces a current proportional to the absolute temperature with a scale factor of 1 μ A/Kelvin. Resistor

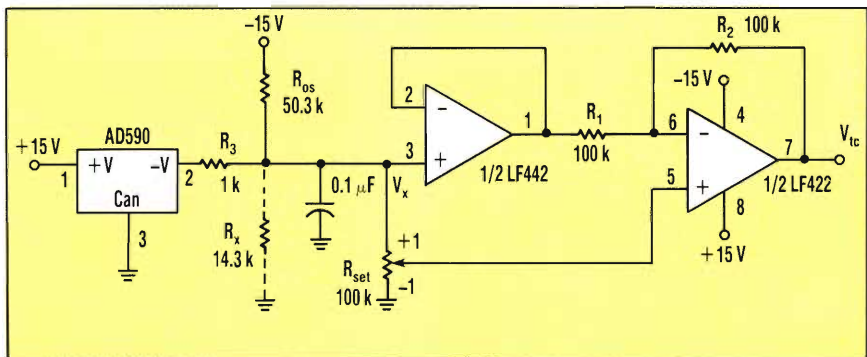
R_{os} and the -15-V supply to which it's connected sink a current equal to the room-temperature AD590 current of 298.2 μ A.

This allows the circuit's operation to be centered at about 25°C (298.2K). Other room-temperature values can be accommodated by simply changing R_{os} .

The maximum magnitude of the circuit's temperature coefficient (V_x) equals the parallel combination of R_{os} , R_{set} , and optional resistor R_x multiplied by the AD590 scale factor of 1 μ A/K. For the values shown in the diagram, including an R_x value of 14.3 k Ω , that maximum magnitude is 10 mV/°C.

Potentiometer R_{set} , resistors R_1 and R_2 , and the two op amps form an

amplifier with a gain that varies linearly from -1 to +1 as the potentiometer wiper moves from bottom to top. That amplifier buffers and scales V_x so that the compensator's output, V_{ic} , can be adjusted over the range of -10 to +10 mV/°C (if R_x is omitted, the range is approximately -33 to +33 mV/°C). □



ALMOST ANY TEMPCO, whether it be positive, negative, or zero, can be set with this inexpensive, simple circuit. For the values shown, the output is zero at 25°C and exhibits a tempco of between -10 and +10 mV/°C depending on the position of the wiper of R_{set} .

CIRCLE
523 ENVELOPE DETECTOR
IS VERY SIMPLE

THOMAS J. SCHUM

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 Herndon, VA 22070; (703) 709-7090.

Among the basic decisions that designers of communications gear and many other types of equipment must make is whether to use envelope detectors or synchronous detectors in

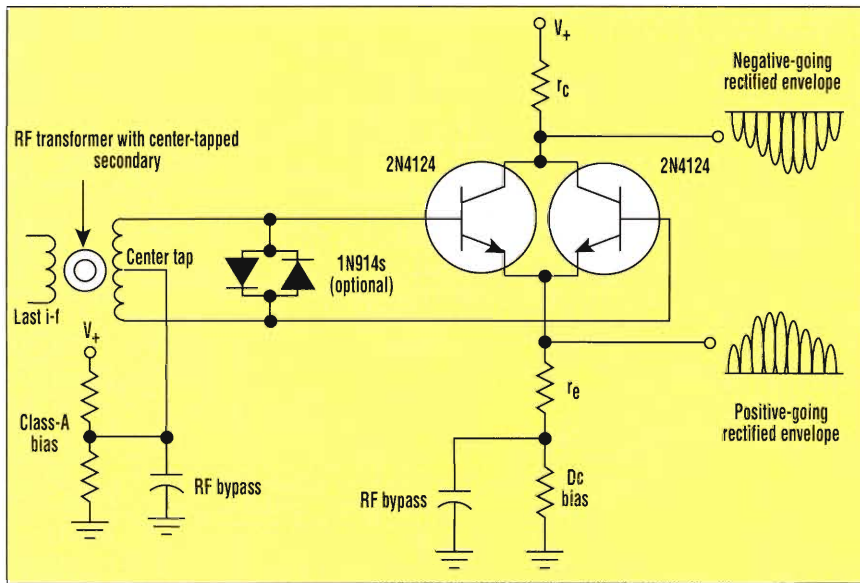
their receivers. Envelope detectors are simpler and less expensive but have non-zero rectification thresholds. Synchronous detectors are more complex yet they offer much higher sensitivity. This two-transis-

tor circuit (see the figure) provides the best of both worlds: It offers the virtually zero rectification threshold of a synchronous detector, but without the complexity.

The circuit is an amplifying full-wave envelope detector that has two transistors connected in parallel except for their bases, which are driven by RF signals that are 180° out of phase. For biasing purposes, the two transistors are treated as a single class-A device.

This method of driving the transistors out of phase with one another has two main effects. First, thanks to emitter coupling between the transistors, this type of detector smooths the portion of the conduction function near the zero crossing, where control passes from one transistor to the other.

Second, due to collector coupling, the circuit eliminates the positive excursions of the output, allowing only the negative half of the amplified



SIMPLE YET SENSITIVE, this amplifying full-wave detector circuit has an almost zero rectification threshold. It presents a highly linear RF load to the final i-f stage. The gain for the collector output is given (approximately) by r_c/r_e . The emitter output gain is slightly less than unity.

detector operates well on low-level signals that are below the base-emitter reverse breakdown voltage of the transistors—typically less than 5 V pk-pk.

Because the detector can amplify, it can be made extremely rugged by keeping the average input voltage below 0.1 V and by placing clipping diodes across the RF input, as shown in the diagram.

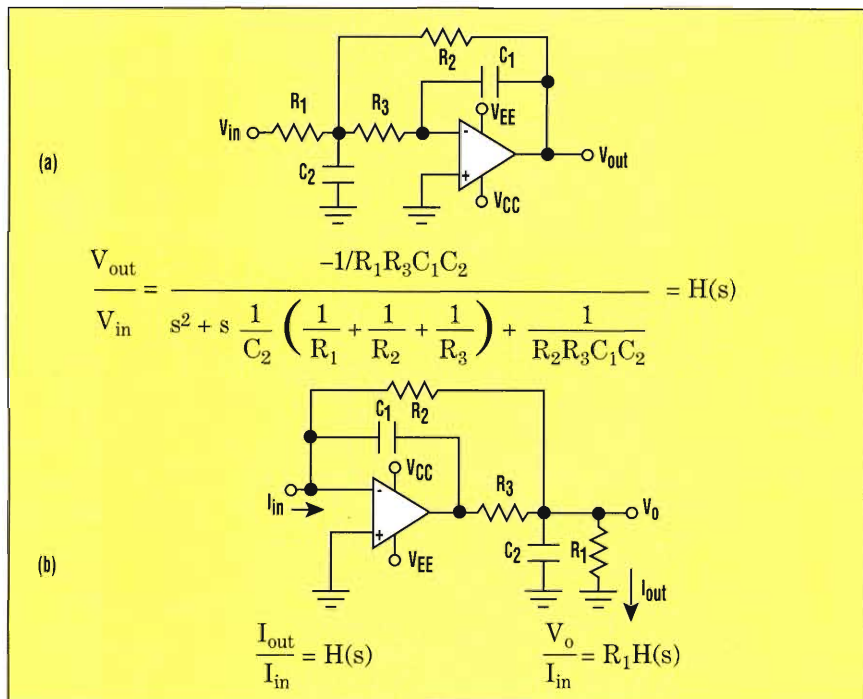
As the RF level goes down, transistor matching becomes increasingly important. However, at normal levels, such as those encountered in conventional diode detector designs, simply using two transistors of the same type is sufficient.

Because the detector threshold is virtually nonexistent, it presents a highly linear RF load to the final i-f stage. That feature, together with the fact that the detector can work with very low level signals, can significantly simplify the design of the last i-f stage. □

523 **SALLEN-KEY FILTER IS CURRENT DRIVEN**

ALFONSO CARLOSENA

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1. THE LOW-PASS SALLEN-KEY filter is staple item for designers because it contains few components (a). By redesigning the filter, a current to voltage conversion can be avoided when the input signal to be filtered is in current form (b).

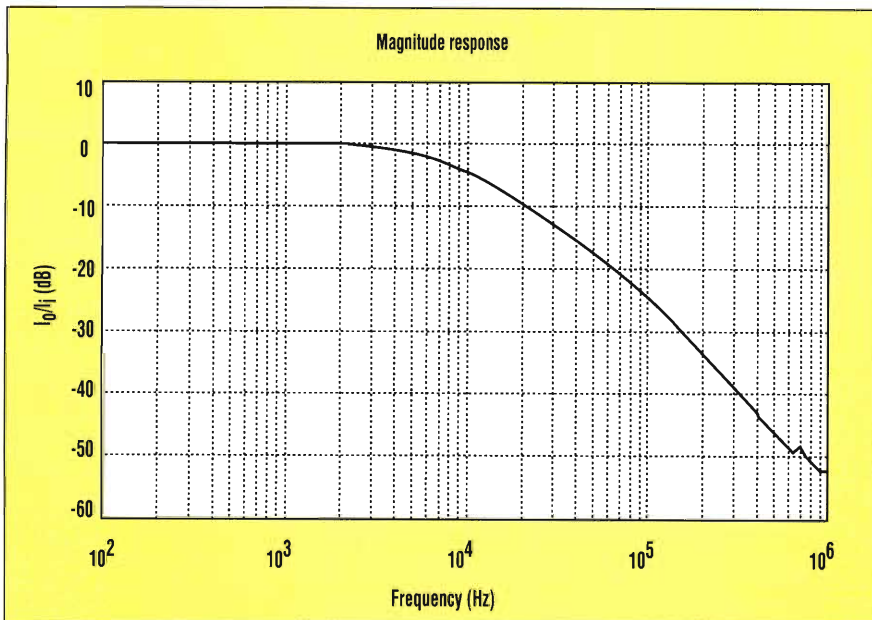
The classic low-pass Sallen-Key filter is very popular among designers because of its minimal amount of passive and active components—2 capacitors, 3 resistors, and 1 op amp (Fig. 1a). At times, though, the input signal to be filtered is in current form (such as when a signal comes from a digital-to-analog converter). In this case, the original structure can be redesigned to avoid a current to voltage conversion.

The new filter (Fig. 1b) accepts currents as input, and the output may be taken in either current or voltage form. The redesign is done with the same components, and without modifying the transfer function (e.g., the voltage transfer function of the original filter is equal to the current transfer function of the modified filter). So, existing tables and design equations can be used.

If a voltage were required at the filter's output, it could be directly obtained from one of the modified circuit's nodes. The transimpedance is then $V_o/I_{in} = R_1 H(s)$.

The filter offers zero input impedance. In addition, it can be cascaded with similar stages by simply connecting the grounded terminal of R_1 to the input of the next stage.

Figure 2 illustrates current frequency response results using a Butterworth filter designed with the Figure 1b scheme. An OP27 op amp was used, as well as the following passive components: $R_1 = 3.16 \text{ k}\Omega$, $R_2 = 3.16 \text{ k}\Omega$, $R_3 = 3.89 \text{ k}\Omega$, $C_1 = 2.2 \text{ nF}$, and $C_2 = 11 \text{ nF}$. □



2. THE CURRENT FREQUENCY RESPONSE of a Butterworth filter, which adopted the redesigned scheme of the Sallen-Key filter, is illustrated. An OP27 op amp and several passive components were used.

CIRCLE 521 LATCHING RELAY IS SOLID STATE

DR. M.J. GEORGE AND T.G. BARNETT

Univ. of London, Queen Mary & Westfield College, Mile End Rd., London, England, E1 4NS; 071 975 5555.

This simple circuit provides a solid state equivalent of the electromechanical latching relay (see the figure). What's more, the switching is clean, highly resistant to vibration and shock, and isn't sensitive to magnetic fields or position.

It was developed because of the need for a latching relay to switch a high-voltage (100 V) pulse generator's output into a load as noiselessly as possible.

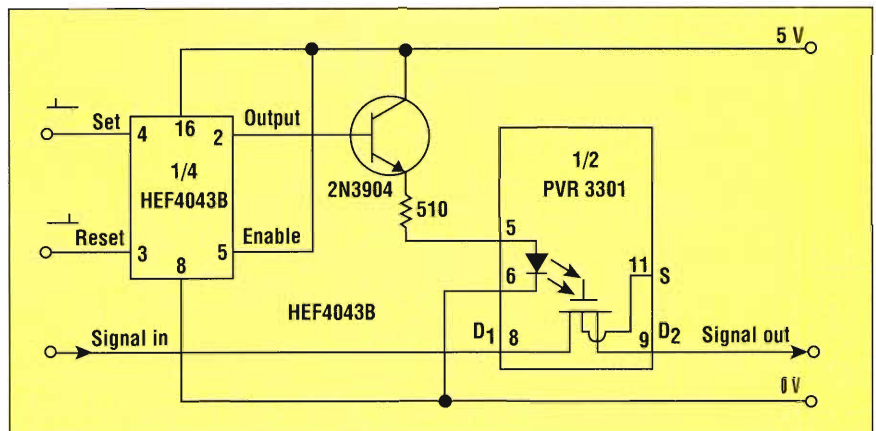
A photovoltaic relay (PVR) was chosen since it allows the control circuitry to be fully isolated. Moreover, it's a low-cost solution to a problem that previously required more complex circuitry.

The PVR combines photovoltaic isolation with a unique bidirectional MOSFET power IC called a BOSFET. Compared to reed relays, PVRs

offer longer life, bounce-free operation, higher operating speeds, and other advantages. In addition, they can switch up to 300 V and several

hundred milliamps.

The circuit operates as follows: A set pulse to the 4043 RS latch takes its output high, turning on the 2N3904 transistor. Current will then flow through the photovoltaic relay's LED and the resistance between D₁ and D₂ will fall from several gigaohms to less than 30 Ω. The PVR will remain in this state until a reset pulse is received by the 4043 RS latch. □



THIS SOLID-STATE LATCHING RELAY employs a photovoltaic relay. The PVR has many advantages, such as longer life span and bounce-free operation. It can also fully isolate control circuitry and is low cost.

CIRCLE 522 SUPPRESS JITTER WITH HYSTERESIS

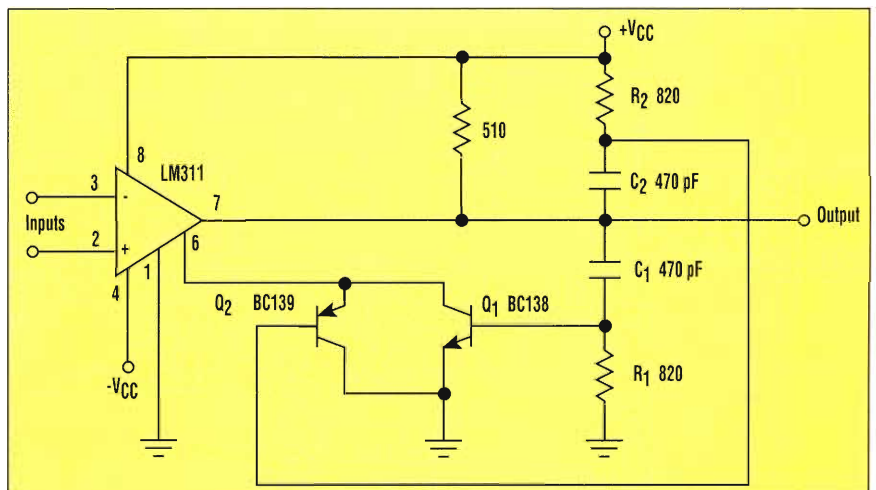
V. SHKARUPIN

P. O. Box 690/4, Kiev-65, Ukraine 252065.

Parasitic jitter at a comparator output, which arises when the input voltages change slowly enough for the comparator to sense the noise component present in the signal, can become a significant problem. Fast comparators are particularly susceptible to such a drawback. Typically, jitter is suppressed by using voltage-domain hysteresis which, though easy to implement, degrades the comparators sensitivity and introduces a delay to the output signal proportional to the hysteresis value.

Another way to tackle the problem is by implementing time-domain hysteresis. That is, the comparator is blocked immediately after its output state changes and this definite state

is sustained for a certain period of time. Like voltage-domain hysteresis, this method uses the positive feedback technique. But unlike the former, time-domain hysteresis doesn't reduce the comparator's sensitivity and won't delay the output



IMPLEMENTING TIME-DOMAIN hysteresis into a comparator is an effective way to suppress parasitic jitter. This circuit diagram shows a comparator with introduced temporal hysteresis. With these elements, hysteresis time is several microseconds.

signal. Time hysteresis is most readily implemented with comparators that have a strobing input, such as the LM311. A comparator with introduced temporal hysteresis is shown (see the figure).

When the comparator's output changes its state from Low to High, the rising edge of the output pulse, differentiated by the C_1 - R_1 chain, opens Q_1 . This blocks comparator M via its strobing input and sustains its output in the H state for a period of

time, defined by the time constant R_1C_1 . After C_1 is charged by the current flowing through R_1 , Q_1 is shut off and the comparator is released. When the comparator's output state changes from High to Low, a similar process, involving elements R_2 , C_2 , and Q_2 , occurs. In many applications, the output transition in only one direction is of vital importance, and the elements, which provide temporal hysteresis for the opposite direction transition, can be omitted. □

CIRCLE 523 BUFFERING SCHEME DRIVES LARGE LCDS

MARTIN TOMASZ

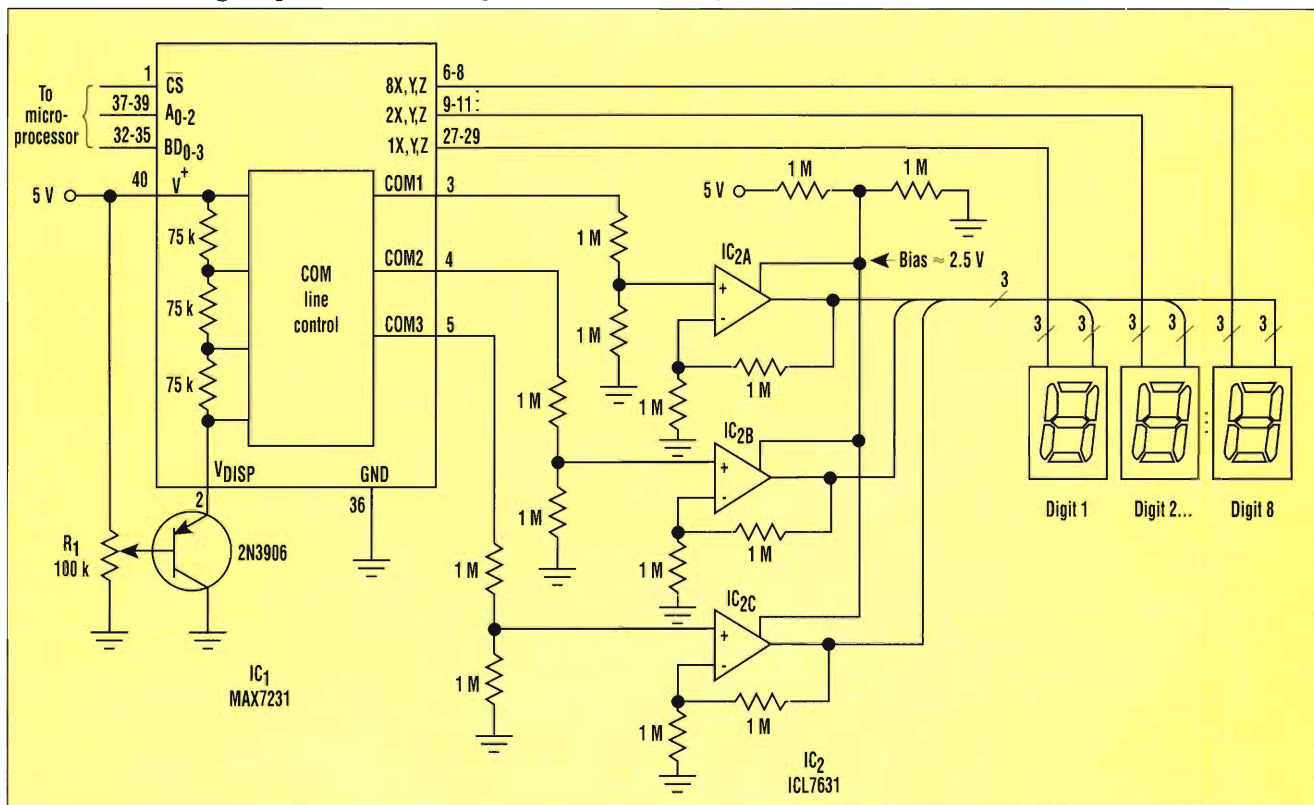
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

To conserve pins, many LCD drivers typically triplex their drive signals. That technique enables ac waveforms on three common lines and three segment lines to activate any standard character of a seven-segment display. However, large LCDs of 1 in. or more exhibit a large capacitance be-

tween the common and segment electrodes (several nanofarads), which presents a problem for standard LCD drivers. The drivers' high output impedance (50 kΩ, for example) causes difficulty in driving capacitance, and the resulting ac-waveform distortion can produce "ghosting" and "shadow" segments in the

display. To solve this problem, the drive circuit shown (see the figure) introduces a buffer amplifier for each of the three common lines. Each amplifier may be programmed independently for a quiescent current of 10, 100, or 1000 μ A. In this application, the bias network applies a voltage that sets the three quiescent currents to 100 μ A.

The display driver and triple op amp operate between 5 V and ground, and the COM signals range from 5 V to ≈ 1 V. To ensure that these signals remain within the amplifiers' common-mode range, the signals are attenuated by one-half and the buffers operate at a gain of two. The circuit drives eight 1-in. displays, and is suitable for ambient temperature variations of 15°F or less. At the highest expected temperature, R_1 should be adjusted so that no "off" segments are visible. □

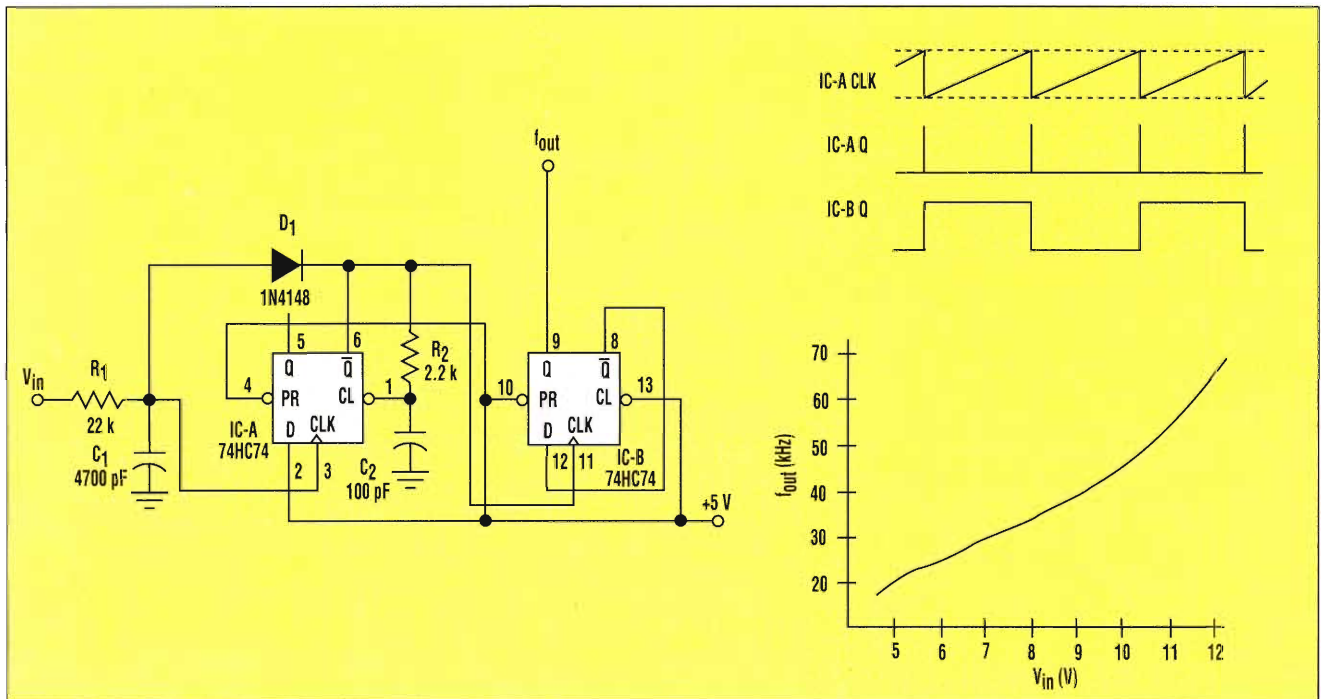


THREE BUFFER AMPLIFIERS enable this standard LCD driver (IC₁) to control eight large (1-in.) seven-segment displays.

CIRCLE
521 DUAL D FLIP-FLOP FORMS VCO

YONGPING XIA
EBT Inc., 2520 W. 237th St., Torrance, CA 90505.

When IC-A's Q output becomes High, C₁ will be discharged through D₁. Meanwhile, IC-A's CL input will also become Low, forcing IC-A to return to Q = Low. The delay due to R₂ and C₂ guarantees that C₁ is discharged before IC-A goes back to Q



A VOLTAGE-CONTROLLED oscillator can be created by using the popular 74HC74 dual D flip-flop. The VCO outputs a 50% duty-cycle square waveform and consumes very low current.

A popular dual D flip-flop (74HC74) can be used to form a voltage-controlled oscillator (see the figure). The circuit outputs a 50% duty-cycle square waveform and consumes very low current. When the input control voltage is between 5 to 12 V,

the output frequency ranges from 20 to 70 kHz.

To illustrate how the circuit works, assume IC-A's initial status is Q = Low. In that case, D₁ is off so that V_{in} charges C₁ through R₁. If the voltage on C₁ reaches a certain level, IC-A will be forced to turn over.

= Low. Obviously, the higher the V_{in}, the larger the charge current for C₁, which means a higher output frequency.

The output produced by IC-A is a stream of very narrow pulses. These pulses trigger IC-B to generate a 50% duty-cycle output signal. □

CIRCLE
522 MULTIPLEX 4-20 MA CURRENT SIGNALS

M. RAILESHA
World Friends, Design Group, 1, 52 Avenue, Kalpakkam 603102,
Tamilnadu, India; tel.: India-(4117)-500.

Generally, 4-to-20-mA signals require independent cables for each signal, with the cables made out of twisted-pair conductors ranging from a few meters to several kilometers in length. One way to simplify that arrange-

ment is by using a multiplexer circuit (Fig. 1). The circuit can replace seven twisted-pair signal lines with a single line.

The circuit consists of eight analog switches driven by a free-running oscillator counter pair, which

ultimately produces a train of 0-to-20-mA output current signals (Fig. 2). As shown, the first analog switch is meant to signal a starting point with no current, and it's used as a synchronization signal to decode the multiplexed information.

The working principle is simple. A free-running oscillator, IC U4A (74HC14), sets the scan rate by adjusting the timing resistor, R₄. The scan clock is counted by a counter, IC U3 (74HC393). The count in the counter finally becomes an address of either one of the 4-to-20-mA analog signals or of zero current. An ad-

CIRCLE 521 WYE-DELTA RECTIFIER REDUCES RIPPLE

JOHN DUNN

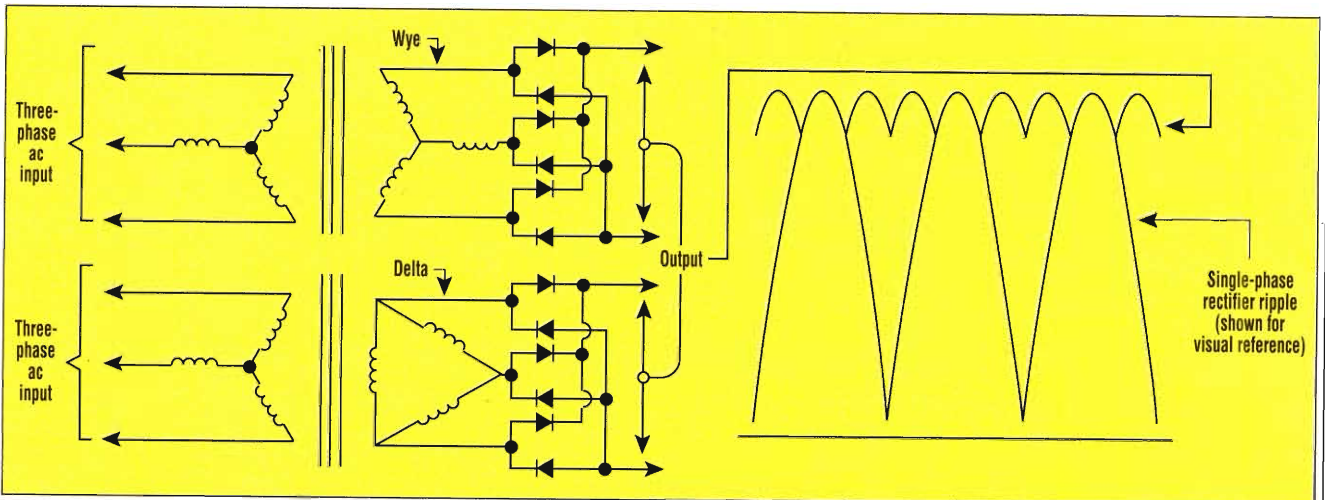
181 Marion Ave., Merrick, NY 11566; (516) 378-2149.

Full-wave rectification from single-phase ac provides an unfiltered rectifier waveform with a dominant ripple frequency twice that of the input line. However, by using a three-phase wye or a delta rectifier, a different full-wave-rectifier waveform is created (Fig. 1). Filtering requirements are thus eased because the dominant ripple frequency is in-

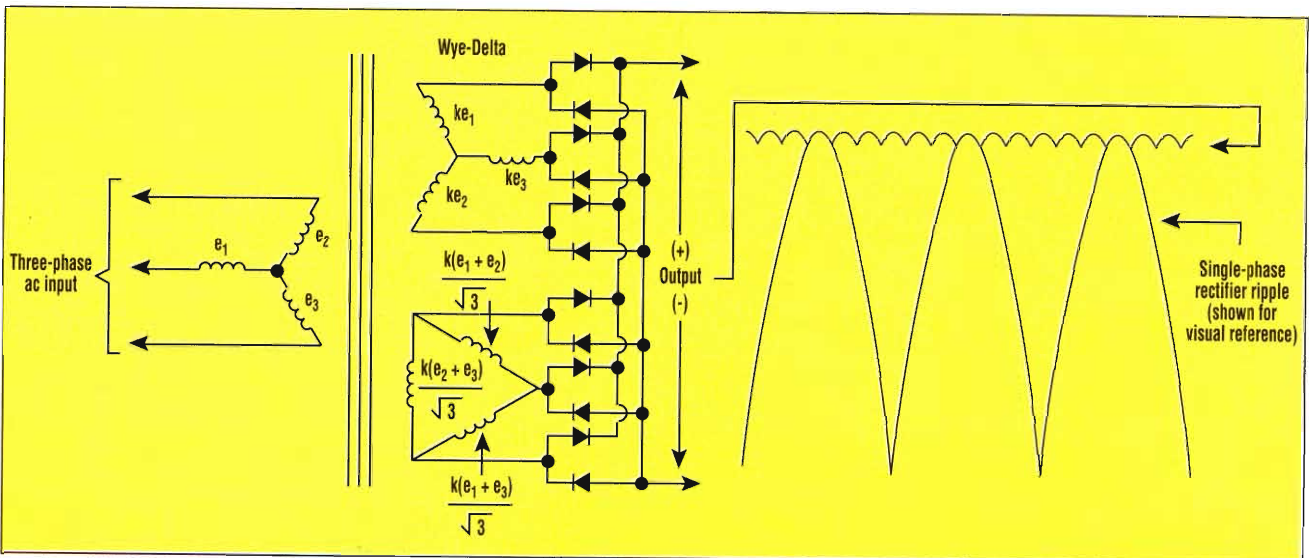
creased to six times that of the input line. It also allows a smaller filter capacitor to be used, thereby minimizing the filter's stored energy—a safety consideration in some applications. If a relatively high rectifier ripple is acceptable, the filter capacitor can be eliminated altogether, reducing the stored energy to zero.

The next step is six-phase rectification with simultaneous wye and

delta rectifiers (Fig. 2). With a transformer having the necessary secondaries, the filtering requirement is easier since the dominant ripple frequency is 12 times that of the input line. And again, depending on the application, the safety hazard of stored energy can be completely eliminated by dispensing with a rectifier filter capacitor—with an even lesser increase of ripple. □



1. A THREE-PHASE WYE or a delta rectifier can provide a full wave rectifier waveform. The dominant ripple frequency is increased to six times that of the input line, thus easing filtering requirements.



2. THIS UNCONVENTIONAL SETUP—six-phase rectification with simultaneous wye and delta rectifiers—makes the filtering requirement even easier than Figure 1. The dominant ripple frequency is raised to that of the input line multiplied by 12.

CIRCLE
522 MODEL FERRITE BEADS IN SPICE

MICHAEL A. WYATT

Honeywell Inc., 13350 U. S. Hwy 19, MS 931-4, Clearwater, FL 34624.

Ferrite beads used for power-supply decoupling represent a difficult modeling problem for those involved in Spice circuit simulations. The bead's frequency-dependent non-linear and non-monotonic behavior are particularly difficult to model. Eventually, the best recourse is to use simple L-R-type equivalent circuit models. But they're only accurate over a narrow frequency range.

Now with the advent of behavioral modeling packages, such as PSpice from MicroSim Corp., accurate modeling and simulation of ferrite beads over a wide frequency range is possible. To model the bead, a voltage-controlled current source (VCCS) behavioral model is used in such a way that the source's terminals appear as an impedance. The source's current is controlled by its terminal voltage as follows:

$$I_{\text{source}} = K(V_{\text{source}})$$

$$Z = V_{\text{source}} / I_{\text{source}}$$

Then:

$$Z = 1/K$$

Thus, the terminal impedance (Z) is the reciprocal of the source's scale factor (K). The listing illustrates this concept for a subcircuit model of the Fair-Rite 2673000101 ferrite bead. GBEAD is the VCCS and is controlled by V(1,2), the source's terminals. FREQ is the behavioral model keyword for a frequency-table-controlled source in PSpice. Data is entered into the table as frequency, magnitude of 1/Z in decibels, and the angle of 1/Z in degrees. Note that the frequency-dependent nonlinear nature of the bead's inductive component would be very difficult to model with discrete circuit elements. If ferrite-bead data is unavailable in an impedance magnitude and angle format, then the impedance magnitude and angle should be computed as:

$$1/Z = \frac{1}{\sqrt{\text{Real}^2 + \text{Img}^2}}$$

$$\angle 1/Z = -\text{Arctan} \frac{\text{Img}}{\text{Real}}$$

MODEL OF THE FAIR-RITE 2673000101 BEAD

```
.SUBCKT BEAD73 1 2
GBEAD 1 2 FREQ {V(1,2)} =
*
+ Freq 1/Z dB 1/Z ang
+ (1k, 40.5, -89.9)
+ (10k, 20.6, -89.5)
+ (100k, 0.9, -80.5)
+ (1meg, -20.4, -59.5)
+ (2meg, -23.4, -46.0)
+ (3meg, -24.7, -39.1)
+ (5meg, -25.4, -36.9)
+ (7meg, -26.2, -35.9)
+ (10meg, -27.7, -34.6)
+ (20meg, -30.0, -23.0)
+ (30meg, -30.3, -16.5)
+ (40meg, -30.0, -12.0)
+ (50meg, -29.7, -08.0)
+ (60meg, -29.6, -06.5)
+ (70meg, -29.6, -06.3)
+ (80meg, -29.6, -06.2)
+ (100meg, -29.6, -06.6)
+ (200meg, -29.7, -09.5)
+ (1000meg, -32.0, -26.0)
RBEAD 1 2 200
.ENDS BEAD73
```

The listing entries are Frequency, 20Log(1/Z), and Angle(1/Z).

Simulation results of the bead's effectiveness on power-supply coupling between two local V_{CC} points fed from a main supply source verified the model's effectiveness.

In another test, the supply network was subjected to a 10-ns, 100-mA current pulse at one V_{CC} point. When the simulation was performed, a time-domain plot showed reduced ringing with the ferrite beads in the circuit.

Some convergence and time-domain simulation problems were ex-

perienced with different bead models. Resistor RBEAD in the listing was included to reduce the Q of the bead and supply a real shunt impedance around the VCCS. RBEAD is determined empirically with the VCCS frequency table coefficients to provide a good representation of the bead's frequency-dependent behavior. □

CIRCLE
523 ELIMINATE RTD SELF-HEATING ERRORS

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Synchronous detection, long used in telecommunications because of performance potential, can now be effectively applied to sensor interface circuitry due to advances in low-cost ICs. This circuit (see the figure) employs a synchronous-detection scheme to measure the resistance of RTDs (resistance-temperature detectors) with self-heating errors of less than 0.001°C.

Conventional circuits require a large current through the sensor so

that the smallest temperature change to be measured results in a voltage change larger than the total system noise, drift, and offset. For example, a 0.3Ω/°C RTD with a 0.1% system resolution requirement and a system offset and drift of only 0.3 mV needs an excitation current in excess of 10 mA. The power dissipated in the RTD causes its temperature to rise above its ambient by:

$$\Delta T = (I^2 R_{\text{RTD}}) \times \theta$$

where ΔT = the change in tempera-

CIRCLE
521 OP AMP DISPELS SHUNT EFFECTS

FRANK T. KOIDE

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The preferred way to do in-circuit measurements when testing and troubleshooting applications is to avoid the removal or decoupling of components from circuit boards. And when it comes to integrated circuits, there's no other way to go. However, in-circuit measurements are not particularly easy to perform.

For example, in the arbitrary network shown in Figure 1, only the integrity of branch 1-2, or impedance Z , is of interest. Conventional measurement of impedance between nodes 1 and 2 obviously includes the effects of the surrounding shunts from node 3 through node 8.

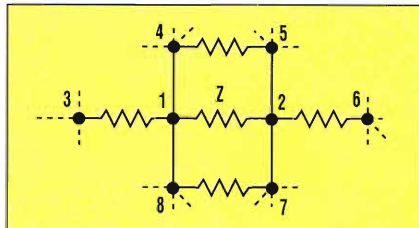
The branch circuit isolator (Fig. 2) can eliminate the effects of the shunts two different ways. First, it maintains adjacent nodes at equipotential, thus preventing currents from flowing through those branches.

Second, it channels only the current from the target branch to flow through the measuring circuit. The latter is achieved by a simple single op-amp current-to-voltage converter, while the former takes advantage of the virtual short-circuit condition of an op amp's input port.

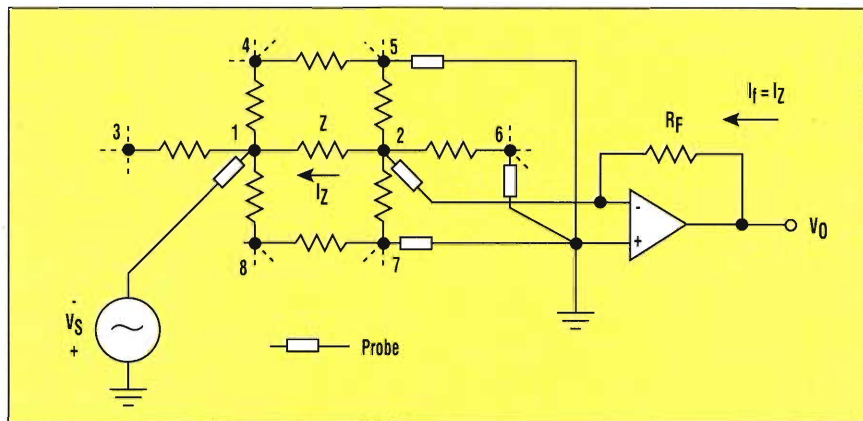
The output voltage V_o is $V_o = I_f R_F$. Because of the virtual short condition that exists at the input to the op amp, the currents flowing from nodes 2 to 5, 2 to 6, and 2 to 7 are zero, and $I_f = I_z$.

Since node 2 is at ground potential, the current flowing through branch Z is:

$$I_z = V_s / Z$$



1. AN ARBITRARY network demonstrates the branch circuit isolator's ability to measure a branch impedance (Z) in a complex circuit without the effects of adjacent shunts.



2. THE BRANCH ISOLATOR CIRCUIT uses a single op amp to measure the impedance between adjacent nodes of a network without having to remove or decouple components.

and the output voltage is:

$$V_o = (R_F / Z) V_s$$

Therefore, the branch impedance that appears between nodes 1 and 2 is defined as:

$$Z = (R_F V_s) / V_o$$

where $(R_F V_s)$ is a constant.

In applications unrelated to electronic testing, the measurement of ionic currents in living tissues and membranes often requires a current that's confined to an area defined by the electrode area, i.e., no fringe currents.

Because the branch circuit isolator, together with guard electrodes, eliminates unwanted currents from the measurement, it's also suitable for voltage-clamp and patch-clamp applications. □

CIRCLE
522 PRESSURE SENSOR CONDITIONS SIGNALS

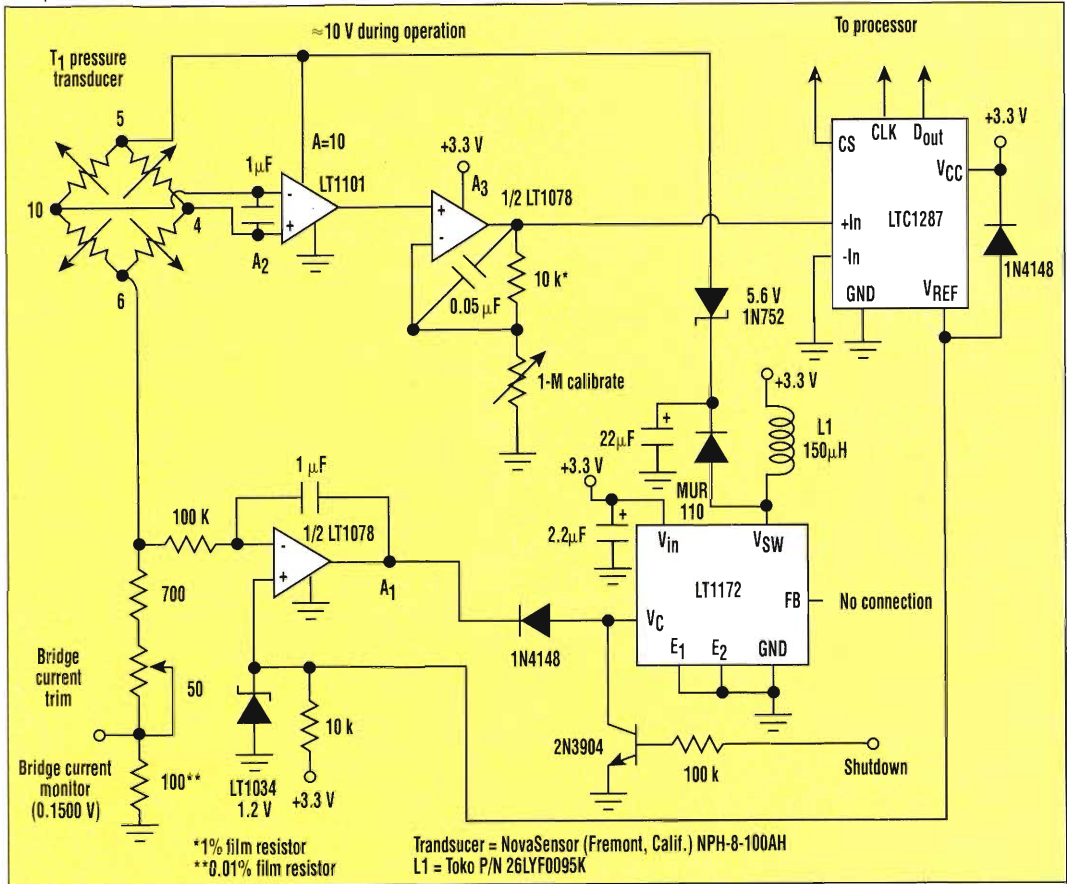
JIM WILLIAMS

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas CA 95035-7487; (408) 954-8400.

The move to 3.3-V digital supply voltage has created problems for analog signal conditioning, particularly for transducer-based circuits that often require higher voltage for proper transducer excitation. In standard configurations, dc-dc converters can address this issue, but they increase

power consumption.

As an alternative, the circuit illustrated (see the figure) offers a way to provide proper transducer excitation for a barometric pressure sensor while minimizing power requirements. The 6-k Ω transducer (T_1) requires precisely 1.5 mA of excitation, thereby necessitating a relatively



14 mA. If the shutdown pin is driven high, the switching regulator shuts down, reducing total power consumption to about 1 mA. In shutdown the 3.3-V-powered ADC's output data remains valid.

The circuit provides a 12-bit representation of ambient barometric pressure after calibration. To calibrate, the "bridge current trim" should be adjusted for exactly 0.1500 V at the indicated point. This sets T₁'s current to the manufacturer's specified point. Then A₃'s trim should be adjusted so that the digital output corresponds with the known ambient barometric pressure. If a pressure standard is unavailable, the transducer is supplied with individual calibration data, permitting circuit calibration. □

THIS CIRCUIT CAN PROVIDE proper transducer excitation for a barometric pressure sensor and at the same time minimize power requirements. This particular 6-k Ω transducer (T₁) needs precisely 1.5 mA of excitation, thus it requires a fairly high voltage drive.

high voltage drive. A₁ senses T₁'s current by monitoring the voltage drop across the resistor string in T₁'s return path.

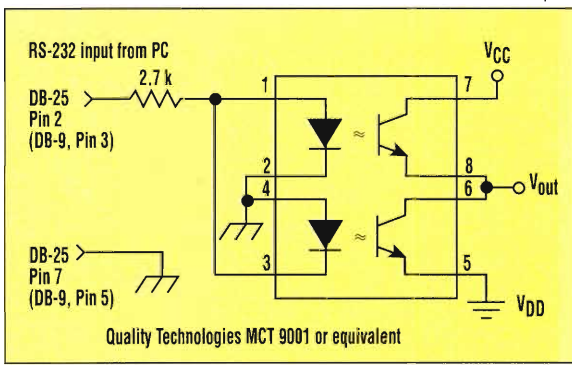
A₁'s output biases the LT1172 switching regulator's operating point, producing a stepped-up dc voltage that appears as T₁'s drive and A₂'s supply voltage. T₁'s return current out of pin 6 closes a loop back at A₁, which is slaved to the 1.2-V reference. This arrangement provides the required high voltage drive (≈ 10 V) while minimizing power consumption. That's because the switching regulator produces only enough voltage to satisfy T₁'s current requirements.

An instrumentation amplifier (A₂ and A₃) provides gain and the LTC1287 analog-to-digital converter supplies a 12-bit output. A₂ is bootstrapped off the transducer supply, enabling it to accept T₁'s common-mode voltage when T₁ is powered. Circuit current consumption is about

CIRCLE 523 PC SERIAL PORT YIELDS SQUARE WAVE

NOOR S. KHALSA
 EG&G Inc., P.O. Box 809, Los Alamos, NM 87544; (515) 667-0200.

By sending an alternative mark/space pattern (55H, ASCII "U") to the serial port on a personal computer, a square wave is generated at the serial out pin. The wave's frequency is 1/2 the baud rate. However, the baud rate can be set to a non-standard value because the UART's two baud-rate divisor registers are user-programmable. The divisor formula is:

$$\text{Divisor} = 1,843,200 / (16 \times$$


THIS CIRCUIT optoisolates the square wave at the RS-232 port and converts the signal to CMOS input voltages.

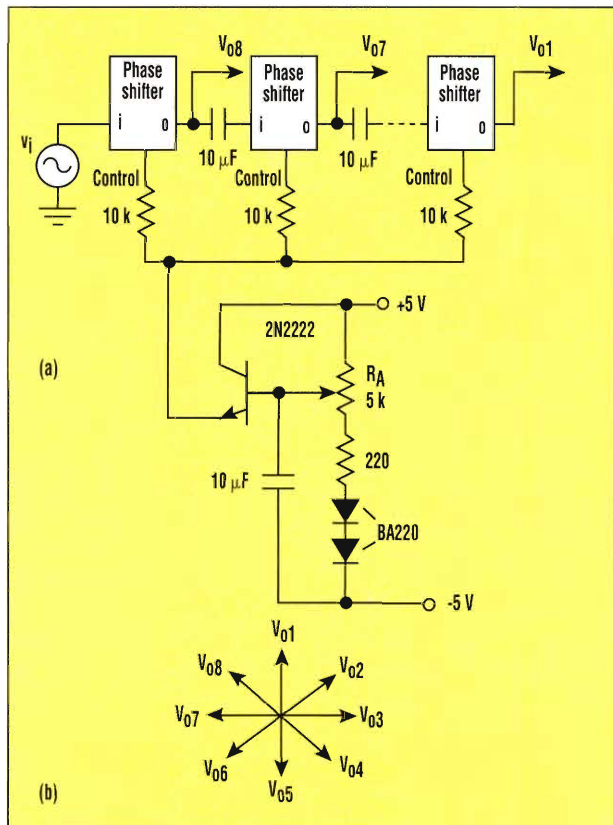
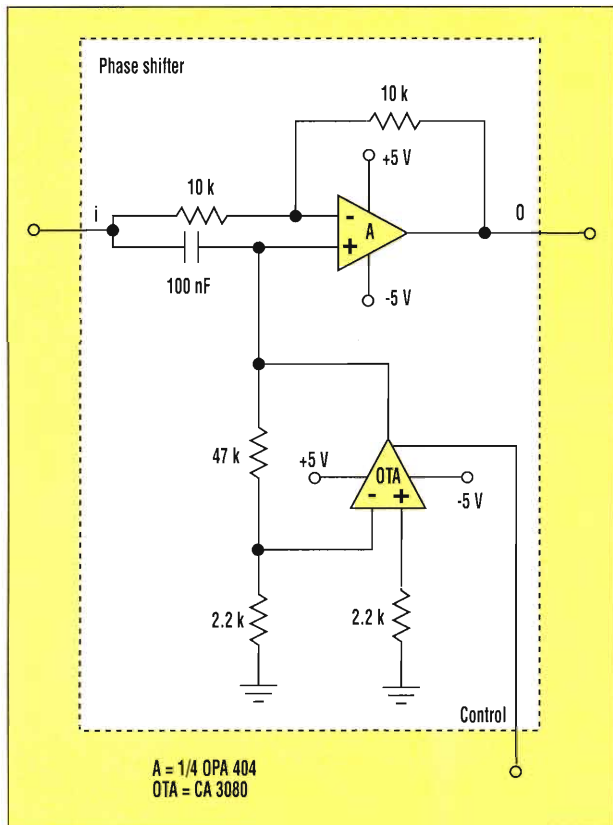
CIRCLE 522 PHASE SHIFTER HAS EIGHT OUTPUTS

ALEXANDRU CIUBOTARU

University of Texas at Arlington, Dept. of Electrical Engineering, Box 19016, Arlington, TX 76019-0016.

shifter will introduce a phase difference of exactly $\pi/4$. The eight signals for PSK are available at the op amps' outputs (Fig. 2b).

Phase accuracy is acceptable for 1%-tolerance resistors and 5%-tolerance 100-nF capacitors. Also, the amplitude of v_i (which is a 1700-Hz sine wave), should not exceed 1 V. □



1. THIS ACTIVE PHASE SHIFTER is one of eight cascaded identical cells used in the overall circuit. Each cell is dc-controlled.

2. THE CIRCUIT IS ADJUSTED by trimming R_A for zero phase difference between v_{o1} and v_i (a). At this point each of the eight outputs will have a phase difference of $\pi/4$ (b).

Here's a cellular phase-shifter circuit that's a key portion of an eight-level PSK (phase-shift keying) transmitter operating at the standard frequency of 1700 Hz. Moreover, by connecting accordingly calculated resistive dividers at some outputs and using buffers, it's possible to obtain a set of signals for QAM (quadrature amplitude modulation).

The circuit consists of eight cascaded identical cells, each cell being a dc-controlled active phase shifter (Fig. 1). Because the dc control is common for all shifters, the circuit is adjusted by trimming R_A (Fig. 2a) so that the phase difference between v_{o1} and v_i is zero. As a result, each

CIRCLE 523 COMPOSITE AMP HAS LOW NOISE, DRIFT

MOSHE GERSTENHABER, MARK MURPHY, and SCOTT WURCER

Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; (617) 935-5565.

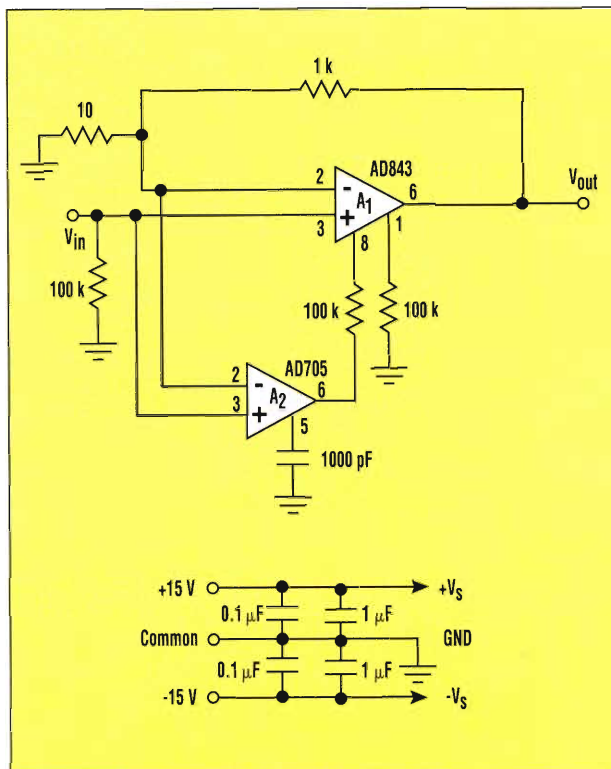
Typically, FET input operational amplifiers have desirable characteristics such as good frequency response, low input bias current, and low input-bias-current noise compared to bipolar input amplifiers.

On the other hand, bipolar operational amplifiers offer such noteworthy characteristics as low input offset voltage, low input-offset-voltage

drift, and low voltage noise.

This composite amplifier circuit (see the figure) offers the best of both worlds. It achieves low current and voltage noise, combined with low input offset voltage and drift, without degrading the overall system's dynamic performance. Compared to a standalone FET input operational amplifier, the composite amplifier circuit exhibits a 20-fold

THIS composite amplifier combines the dc precision of a bipolar amplifier with the dynamics of a high-speed FET amplifier. Low current and voltage noise, as well as low input offset voltage and drift, are attained without degrading dynamic performance.



improvement in voltage offset and drift.

In this circuit arrangement, A₁ is a high-speed FET input op amp with a closed-loop gain of 100 (the source impedance was arbitrarily chosen to be 100 k Ω). A₂ is a Super β bipolar input op amp. It has good dc characteristics, biFET-level input bias current, and low noise. A₂ monitors the voltage at the input of A₁ and injects current to A₁'s null pins. This forces A₁ to have the input properties of a bipolar amplifier while maintaining its bandwidth and low input-bias-current noise. □

CIRCLE
521 FILTER HAS FOUR OUTPUTS

YISHAY NETZER
Yuvalim 112, Israel 20142.

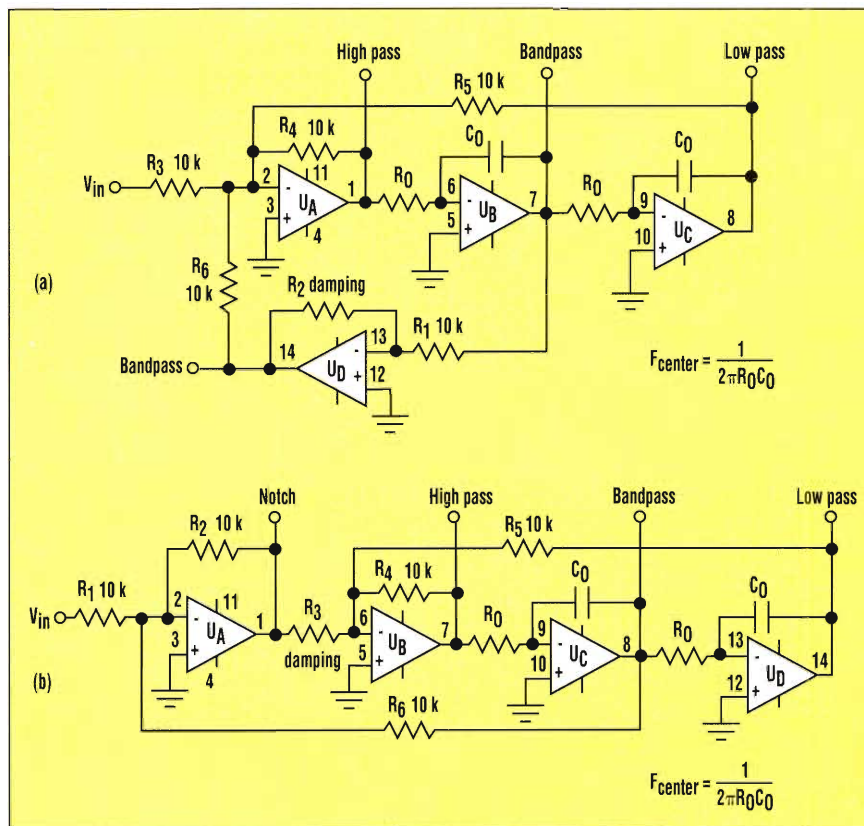
The classical "state-variable" (two-integrator) filter (see the figure, a) is famous for its insensitivity to device parameter tolerances, as well as its ability to provide three simultaneous separate outputs: high pass, bandpass, and low pass. These advantages often offset the fact that a quad operational amplifier is needed to implement the circuit.

A modification of the classical scheme that applies the input voltage via amplifier U_D rather than U_A provides a bandpass output with a fixed peak gain that doesn't depend on the Q of the filter.¹ It was found by employing that configuration, a fourth notch-filter output can be obtained if $R_1 = R_6$ (see the figure, b).

If $R_1 = R_6 = R_2$, the gains of both the notch and bandpass outputs are unity, regardless of the Q factor, as determined by $R_3, R_4, R_5,$ and R_6 are preferably of a monolithic resistor network. The resonant (or cutoff) frequency is given by $\omega = 1/R_0 \times C_0$. Depending on the capacitor values and the frequency ω , the resistors R_0 may also share the same monolithic network for maximum space economy. As with the classical

configuration, the resonant frequency ω can be electronically controlled by switching resistors R_0 , or by employing analog multipliers in series with the integrators. □

¹Bernie Hutchins, "Filter's Gain Is Independent Of Q ," EDN, Nov. 24, 1982.



THE CLASSIC state-variable filter is well regarded for its insensitivity to device parameter tolerances, and that it can provide three simultaneous outputs (a). By modifying the classic filter, a fourth notch-filter output can be obtained (b).

CIRCLE
522 RECTIFIER HAS NO DIODES

SERGEY KUNIN

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It's common knowledge that when working with single-supply op amps, implementing simple functions in a bipolar signal environment can be difficult. Sometimes additional op amps and other electronic components are required.

Taking that into consideration, can any advantage be attained from this mode? The answer lies in this simple circuit (see the figure, a). Requiring

no diodes, the circuit is a high-precision full-wave rectifier with a high-frequency limitation equaling that of the op amps themselves. A look at the circuit's timing diagram (see the figure, b) illustrates the principle of operation.

The first amplifier rectifies negative input levels with an inverting gain of 2 and turns positive levels to zero. The second amp, a noninvert-

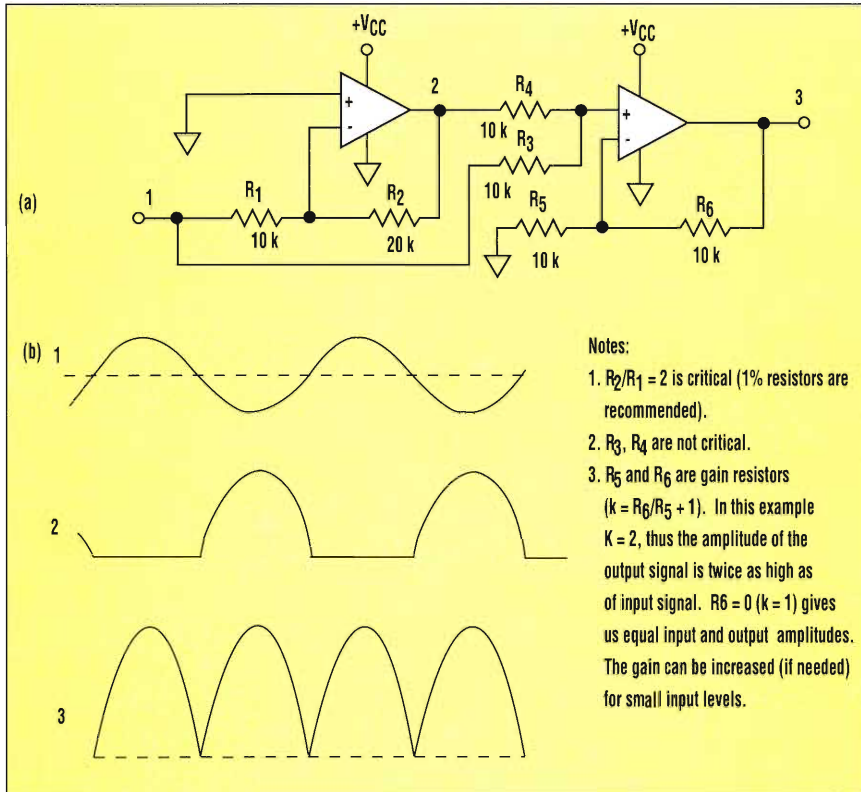
IFD WINNER

IFD Winner for
November 12, 1992

Noor S. Khalsa, EG&G Inc., P.O. Box 809, Los Alamos, NM 87544; (515) 667-0200. His idea: "PC Serial Port Yields Square Wave."

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Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a \$150 Best-of-Issue award and becomes eligible for a \$1,500 Idea-of-the-Year award.



- Notes:
1. $R_2/R_1 = 2$ is critical (1% resistors are recommended).
 2. R_3, R_4 are not critical.
 3. R_5 and R_6 are gain resistors ($k = R_6/R_5 + 1$). In this example $k = 2$, thus the amplitude of the output signal is twice as high as of input signal. $R_6 = 0$ ($k = 1$) gives us equal input and output amplitudes. The gain can be increased (if needed) for small input levels.

1. THIS SIMPLE CIRCUIT, built around two sections of an LM2902 quad op amp, is actually a high-precision full-wave rectifier that requires no diodes (a). Rectification is accomplished by summing with the input signal, the negative signal excursions which have been inverted and amplified by a factor of 2 (b).

ing summing amplifier, adds the inverted negative signal from the first amplifier to the original input signal. The net result is the traditional waveform produced by full-wave

rectification.

In spite of the limitation on the input signal amplitude (it must be less than $V_{CC}/2$), this circuit can be useful in a variety of setups. □

CIRCLE 523 CURRENT SOURCE ADJUSTS FOR OFFSET

JOHN STOUGHTON

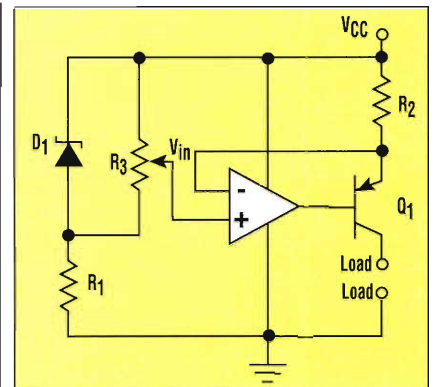
United Medical Manufacturing Co., 6911 Hillsdale Court, Indianapolis, IN 46250.

By carefully choosing components, you can create a cost-effective circuit for a current source with an output that's accurate to 1% (Fig. 1). I_{out} (the current flowing from the collector of Q_1) is $V_{CC} - V_{in}$ (the voltage at the wiper of R_3) divided by the value of R_2 .

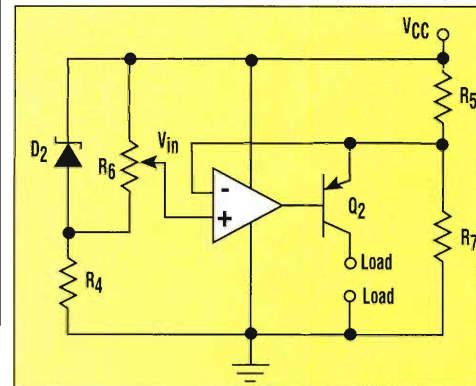
In some instances, it's important to be able to turn off the current source (within the limits of I_{CEO} for Q_1). Unfortunately, in about half of these cases, the offset voltage (V_{OS}) of the op amp will turn the current

source on even when $V_{CC} = V_{in}$. That's because the offset voltage (when the noninverting input needs to be at a higher potential than the inverting input to get an output of 0 V from the op amp) is impressed across R_2 . This offset voltage forces Q_1 to turn on enough to yield a collector current of V_{OS} divided by R_2 .

Figure 2 offers a fix for this predicament. The addition of R_7 presents the emitter of Q_2 with a Thévenin equivalent voltage and resistance represented by:



1. THOUGH this setup can act as a cost-effective current source with an output accurate to 1%, the voltage offset will turn on the current source even when V_{CC} equals V_{in} .



2. MODIFYING the configuration of Figure 1 can rectify the problem of the current source being turned on by the voltage offset. The addition of R_7 allows an adjustment that guarantees turn-off for any op-amp offset specification.

$$V_{TH} = V_{CC}[1 - (R_5/R_5 + R_7)]$$

$$R_{TH} = (R_5 \times R_7)/(R_5 + R_7)$$

The difference between V_{CC} and V_{TH} is $V_{CC}(R_5/R_5 + R_7)$. If $V_{CC}(R_5/R_5 + R_7)$ is set equal to the maximum V_{OS} spec for the op amp in question, the circuit is then guaranteed to turn off. This circuit has an output current of $V_{TH} - V_{in}$ divided by R_{TH} .

The compromise of Figure 2 does present another error term in the circuit. The term $(V_{TH} - V_{in})$ will have to be $2 \times V_{OS}$ to guarantee a current output for the whole population of the op amp chosen. This error can be made arbitrarily small (but not zero) by increasing the voltage of D_2 and V_{CC} , while also raising the value of equivalent resistance R_{TH} . □

CIRCLE 521 FAST COMPOSITE AMP HAS LOW DISTORTION

SCOTT WURCER and CHARLES KITCHIN
Analog Devices Inc., P.O. Box 9106, Norwood, MA 02602.

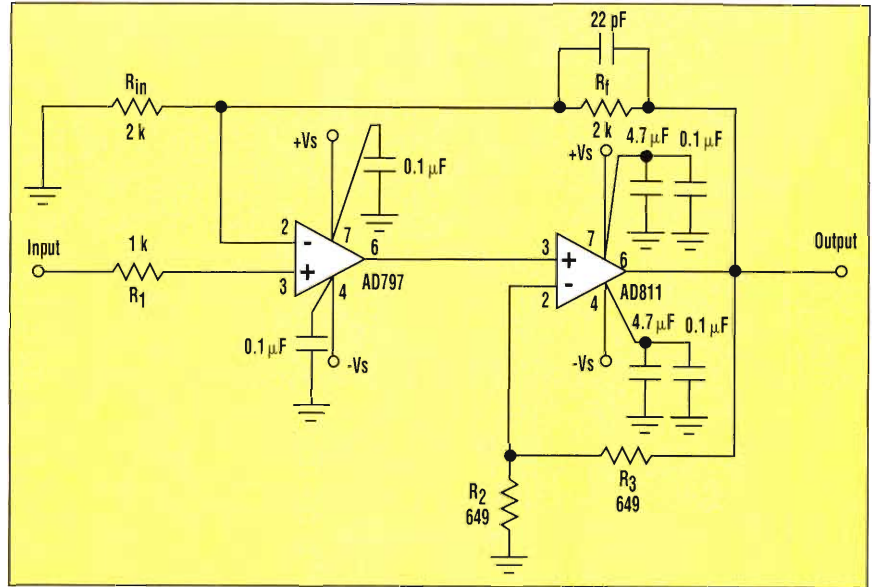
Although current feedback op amps offer high bandwidths over a wide range of closed-loop gains, they do have limitations. For instance, they typically have larger input offset errors and higher distortion at low gains than do comparable voltage feedback amplifiers.

By combining two op amps in a composite amplifier configuration, this circuit (see the figure) can overcome those disadvantages and achieve high performance. Here, an ultra-low-noise, low-distortion op amp—the AD797—is combined with the AD811 op amp, which offers a high bandwidth and a 100-mA output drive capability. The composite-amplifier circuit serves quite well when driving high-resolution ADCs and ATE systems.

The fast AD811 operates at twice the gain of the AD797 so that the slower amplifier need only slew one-half of the total output swing. Using the component values shown, the circuit is capable of better than -90 dB THD with a ± 5 -V, 500-kHz output signal. If a 100-kHz sine-wave input is employed, the circuit will drive a 600- Ω load to a level of 7 V rms with less than -109 dB THD, as well as a 10-k Ω load at less than -117 dB THD.

The device can be modified to supply an overall gain of 5 by changing both the R_F/R_{in} ratio and R_3/R_2 ratio to 4:1. This raises the gains of AD811 and the total circuit while maintaining the AD797 at unity gain. If only the R_F/R_{in} ratio is changed, the cir-

cuit may become unstable. In contrast, if only the R_3/R_2 ratio is varied, the AD797 will then operate at gain. Subsequently, the circuit will have a lower overall bandwidth. R_1 should be equal to the parallel combination of R_{in} and R_F . □



A COMPOSITE amplifier with an ultra-low distortion can be created by combining two op amps, which in this case are the AD797 and AD811. With the given component values, the circuit is capable of a -90 dB THD with a ± 5 -V, 500-kHz output signal.

CIRCLE 522 CHOP DC OUTPUT TO GET AC STANDARD

M.J. SALVATI
Flushing Communications, 150-46 35th Ave., Flushing, NY 11354.

Voltage standards for ac are rarely found outside a metrology lab. However, a crude yet effective way to rig a source of known ac voltage is to chop the output of a known dc voltage source. Either a dc voltage standard or a stable dc supply monitored by a 4-digit DVM can be used as the source of known dc voltage.

Any dc voltage source in the 2-to-15-V range can be chopped into a unipolar square wave that has a peak amplitude nearly equal to the dc source voltage with this circuit (lightly loaded CMOS will

swing within a few millivolts of each rail at low frequencies) (see the figure on p. 94).

Depending on the actual voltage of the supply, the programmable-unijunction-transistor (PUT) relaxation oscillator produces 1600-2000 Hz trigger pulses. These pulses operate the cascaded 74C107 flip-flops, producing a square wave whose fre-

IFD WINNER

IFD Winner for
January 7, 1993

Mike McNatt, Amoco Technology Co., P.O. Box 3011, Naperville, IL 60566-7011; (708) 961-6296. His idea: "One Pot Adjusts Polarity, Gain."

INTERNAL METER COUPLING

Meter rectifier type	DC	AC
Average responding	2.000	2.000
Average responding, rms calibrated	1.800	1.800
True rms	1.414	2.000
Peak	1.000	2.000

CIRCLE
521 BUILD 110-DB BEEPER CIRCUIT

DAVID A. JOHNSON
10198 W. Berry Dr., Littleton, CO 80127.

Most piezoelectric beeping devices with internal drivers lack sound intensity, only producing about 80 dB when powered from a 9-V battery. If more sound is required, this circuit will generate an ear-splitting 110 dB from 9 V (see the figure).

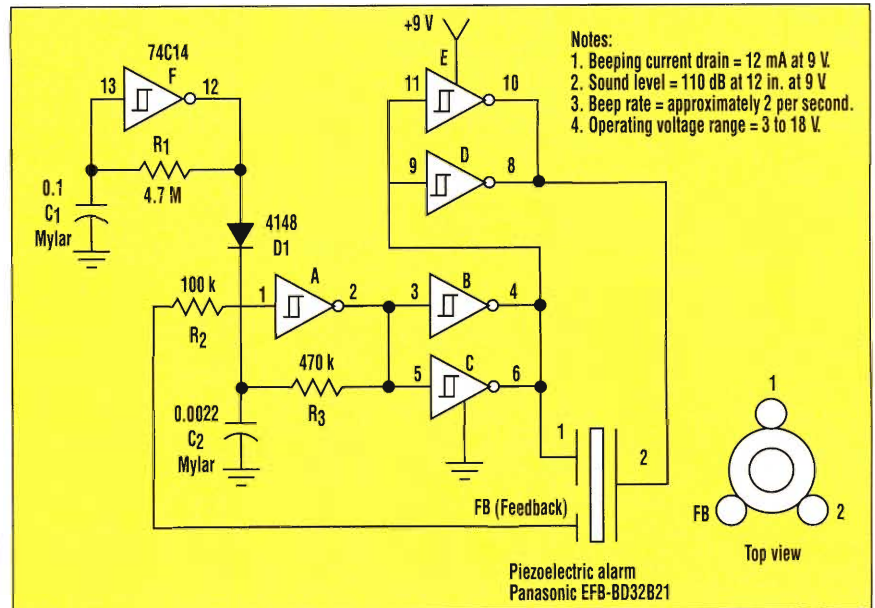
The setup employs a single 74C14 (CD40106B) CMOS hex inverting Schmitt-trigger IC, which must be used with a piezoelectric device with a feedback terminal. The feedback terminal is attached to a central region on the piezoelectric wafer. When the beeper is driven at resonance, the feedback signal peaks.

One inverter of the 74C14 is wired as an astable oscillator. The frequency is chosen to be about 5 times lower than the 3.2-kHz resonant frequency of the piezoelectric device. Feedback from the third pin of the beeper reinforces the correct drive frequency to ensure maximum sound output.

Four other inverter sections of the

IC are wired to form two separate drivers. The output of one section is

cross-wired to the input of the second section. The differential drive signal that results produces about 18 V p-p when measured across the beeper. The last inverter section is wired as a second astable oscillator with a frequency of about 2 Hz. It gates the main oscillator on and off through a diode. For a continuous tone, the modulation circuit can be deleted. □



THIS beeper-circuit setup can generate 110 dB from 9 V. It uses a single 74C14 CMOS hex inverting Schmitt-trigger IC along with a feedback-terminal-equipped piezoelectric device.

CIRCLE
522 FILTER USES SYNTHETIC INDUCTOR

GARY SELLANI
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086;
(408) 737-7600.

Inductors have a bad reputation as filter components—not only do they transmit electromagnetic interference, but they also act as antennas for receiving EMI signals generated elsewhere.

To avoid these problems, you can simulate an inductor's impedance by combining two wideband transconductance amplifiers (WTAs) and a capacitor (Fig. 1a). The combined circuit then acts as a synthetic inductor (L_{SYN}) with one end connected to ground.

By forcing current at L_{SYN} and measuring the resulting voltage, you can determine the equivalent im-

pedance Z_{EQ} of the circuit:

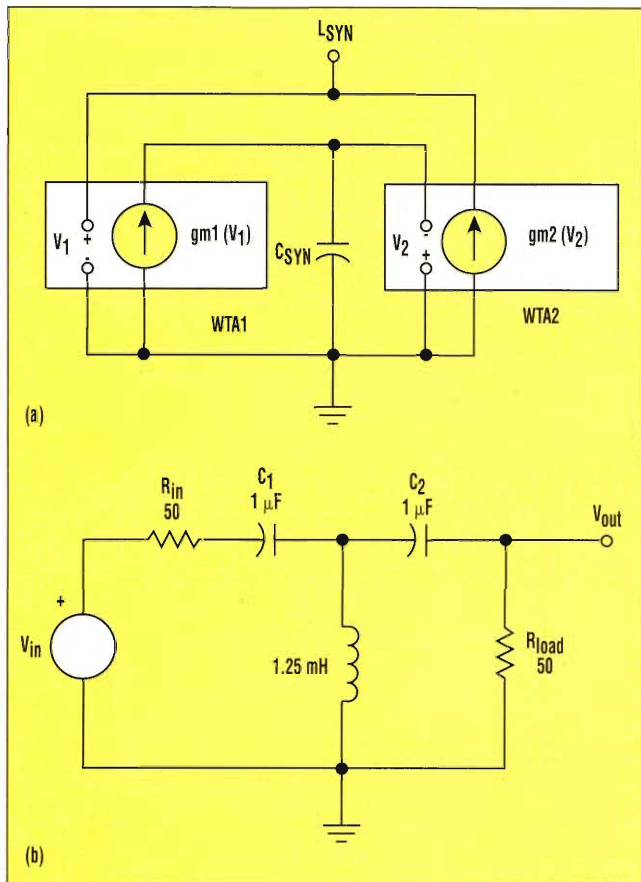
$$Z_{\text{EQ}} = \omega C_{\text{SYN}} / gm1 \times gm2$$

where gm = transconductance

The equivalent inductance, therefore, is:

$$L_{\text{EQ}} = C_{\text{SYN}} / gm1 \times gm2$$

This single-port network clearly offers the frequency-proportional impedance of an inductor, and the inductance value can be large if $gm1 \times gm2$ is much less than 1. The only limitation is that the network must always connect to ground.



1. THIS SINGLE-PORT network simulates an inductor with two wideband transconductance amplifiers and a capacitor (a). A good application for the simulated inductor is the simple ladder filter (b). It must have one end connected to ground.

High-pass, all-pole ladder filters make good applications because all of their inductors connect to ground. Two WTAs and a capacitor must be substituted for each one, so you should choose a configuration with the minimum number of inductors.

To be cost-effective, your design should feature a series capacitor at each end of the filter, with the simulated inductor acting as a shunt between them (Fig. 1b). The input capacitor blocks any dc applied to the filter, and the output capacitor blocks any dc offset introduced by the synthetic inductor. Though constructed with active components, the filter does retain some of

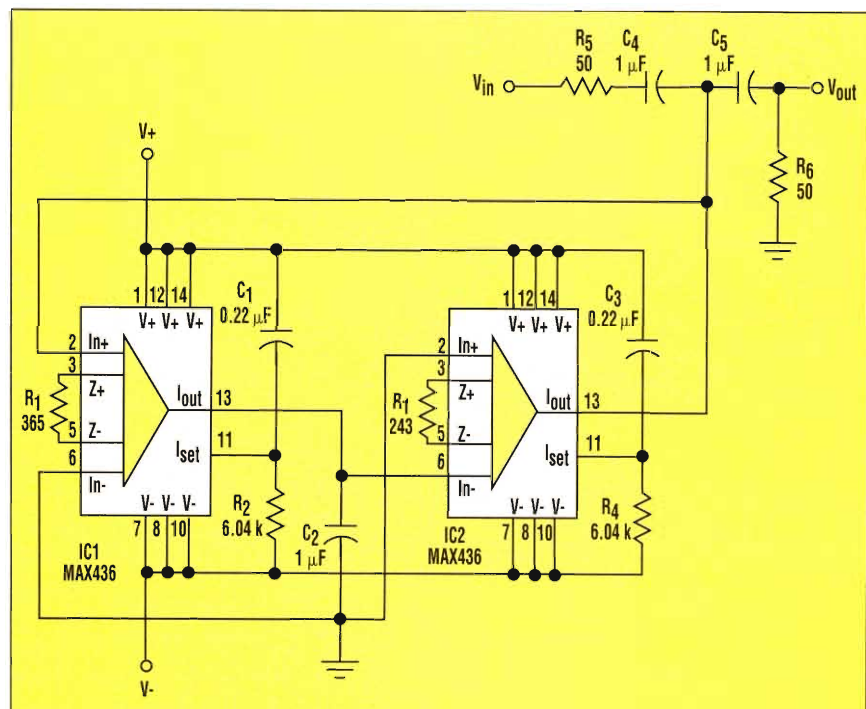
the advantages of a passive filter.

In an actual circuit (Fig. 2), C_1 and C_3 become bypass capacitors and C_2 is part of the simulated inductor. The transconductance for each WTA is set by an external resistor (R_1 or R_3) according to the relationship $gm = 8/R$ (where $R = R_1$ or R_3). Because the simulated inductance depends on the product of these transconductances, it may appear that you have a range of choices for each. But the optimum circuit for a given application restricts gm values by allowing the full range of output swing for each WTA.

To determine these optimal gm values, start with equal transconductance and simulate the filter in Spice using "g" elements (voltage-controlled current sources) for the amplifiers. While sweeping the frequency at least one decade above and below the filter's corner frequency, observe each WTA output for its peak voltage magnitude (the two peaks may occur at different frequencies).

At the synthetic inductor's port (pin 13 of IC2), the peak value is demanded by the filter and can't be changed. A real inductor would produce the same peak. Therefore, you adjust the other peak to match. Let K equal the ratio of gm_2 to gm_1 , and then, since gain is proportional to transconductance, you divide gm_1 by K and multiply gm_2 by K . Finally, rerun the Spice simulation with these new gm values to verify that the peaks are equal and that the filter shape has not changed.

The filter exhibits a maximum attenuation of 58.6 dB/decade. The slope decreases at lower frequency because the synthetic inductor's Q is affected by its series resistance (comparable 1.25-mH inductors also have an appreciable resistance of 53 Ω or so). At 10 Hz, for instance, the attenuation for an ideal filter is -90 dB. For this circuit, the attenuation is -80 dB. \square



2. A 3RD-ORDER

BUTTERWORTH high-pass filter is constructed by substituting the simulated inductor of Figure 1a in the ladder filter of Figure 1b. The filter has a 3.2-kHz corner frequency and a -6-dB loss due to the source and load impedances.

CIRCLE 521 CREATE EFFICIENT LASER POWER SUPPLY

JIM WILLIAMS

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487.

Helium-neon lasers are useful in a variety of tasks, but they're difficult loads for a power supply to handle. Powering a laser usually involves some form of startup circuitry to generate the initial breakdown voltage and a separate supply to sustain conduction. Typically, almost 10 kV is needed to start conduction, and about 1500 V is required to maintain conduction at their specified operating current. The circuit shown considerably simplifies driving the laser (see the figure). The startup and sustaining functions are combined into a single closed-loop current source with over 10 kV of compliance.

When power is applied, the laser doesn't conduct and the voltage across the 190- Ω resistor is zero, and the LT1170 switching-regulator "FB" pin observes no feedback voltage. Therefore its switch pin (V_{SW}) provides full duty-cycle pulse-width modulation to L_2 . Current flows from L_1 's center tap through Q1 and Q2 into L_2 and the LT1170. This flow causes Q1 and Q2 to switch, alternately driving L_1 .

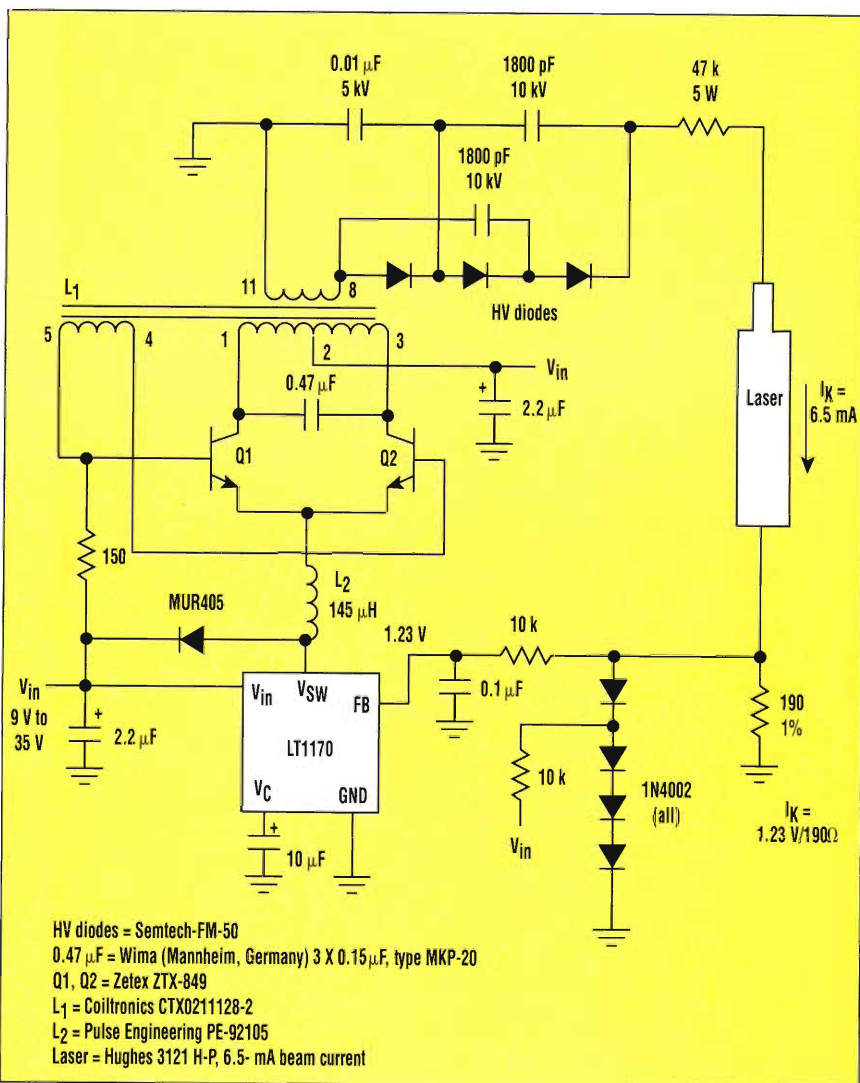
When the 0.47- μ F capacitor resonates with L_1 , it supplies boosted sine-wave drive. L_1 provides substantial step-up, which causes about

3500 V to appear at its secondary. The capacitors associated with L_1 's secondary form a voltage tripler, producing over 10 kV across the laser. The laser breaks down and current begins to flow through it.

The 47-k Ω resistor ballasts the laser, which limits current. That current flow causes a voltage to appear across the 190- Ω resistor. A filtered version of this voltage appears at the

LT1170 FB pin and subsequently closes a control loop. The LT1170 adjusts its pulse-width drive to L_2 to maintain the FB pin at 1.23 V, regardless of changes in operating conditions. The laser can then see constant current drive, which in this case is 6.5 mA. Other currents are obtainable by varying the 190- Ω value.

The 1N4002 diode string clamps the voltage when laser conduction begins, protecting the LT1170. The 10- μ F capacitor at the V_C pin frequency compensates the loop. The MUR405 maintains L_2 's current when the V_{SW} pin isn't conducting. The circuit starts and runs the laser over a 9-to-35-V input range with about 75% electrical efficiency. □



DRIVING HELIUM-NEON LASERS can be simplified considerably using this power-supply configuration. When power is applied, the laser doesn't conduct and the voltage across the 190- Ω resistor is zero. However, a resonant circuit and a voltage tripler then produce over 10kV to turn on the laser.

CIRCLE 521 SWITCHING BOOST REGULATOR USES 555

DAVID LAUDE
7040 Franciville Rd., Colorado Springs, CO 80908.

While working on a "B" battery replacement for antique battery-powered radios, it occurred to me that the venerable 555 timer might be able to handle most of a switching regulator's task. This circuit does just that (see the figure).

During operation, C_1 is alternately charged and discharged. Resistor R_1 ensures that C_1 begins charging. It also sets the minimum switching frequency. While C_1 is charging, pin 3 of the 555 timer drives Darlington pair Q1-Q2 to supply current to the inductor. When the inductor current reaches a value determined by R_2 and Q3's base-emitter turn-on voltage, the collector current of Q3 will rapidly charge C_1 .

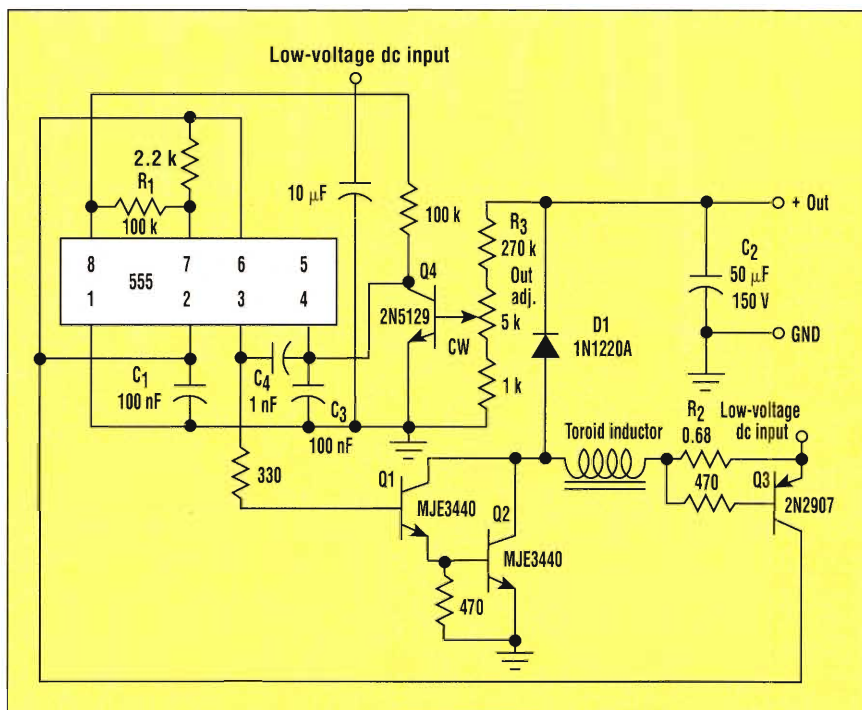
When the voltage across C_1 reaches the point where the 555 will reset, the voltage on pin 3 will go low, turning Q1-Q2 off. This action saves from consuming more power than is needed from the supply. At the same time, pin 7 will begin to discharge C_1 . During this turn-off event, the collector voltage of Q1-Q2 will be pulled high by the inductor's flyback action. Diode D1 steers the inductor current into storage capacitor C_2 . When C_1 's discharging voltage reaches the set threshold, pin 3 again goes high to repeat the cycle.

Output-voltage regulation is accomplished by monitoring the voltage across C_2 . Whenever Q4 turns on (an indication of excess output voltage) the collector pulls the 555's reset pin low. This turns off the drive to Q1-Q2 until the output voltage drops slightly. C_3 provides low-pass filtering to help the circuit remain stable during regulation. When pin 3 switches low, C_4 provides hysteresis to pin 4 for added stability.

The component values shown, chosen from my junk box, worked well to supply 80 V at 10 mA from a 7.5-V input with about 60% efficiency. The toroid's inductance is several hundred microhenries. R_3 can be modi-

control electronics will help to maximize performance. An additional capacitor, connected across pins 1 and 5 of the 555, will help reduce the influence of supply noise.

The circuit will exhibit some temperature drift due to the base-emit-



THIS 555-TIMER-BASED CIRCUIT can function as a switching regulator. With the component values shown, the device supplied 80 V at 10 mA from a 7.5-V input with about 60% efficiency.

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ter turn-on voltages of Q3 and Q4 being used as reference voltages. The device works very well in uses around the home or in the shop. □

CIRCLE 522 RUN OPTOISOLATOR AT 100 kHz, LOW POWER

B.R. BEER
Fisons Instruments, Floats Rd., Wythenshawe,
Manchester, United Kingdom M23 9LE.

This circuit can drive an inexpensive optocoupler with high voltage isolation at frequencies above 100 kHz using an AD654 voltage-to-frequency converter. The AD654 provides an open collector output with 50% conduction duty cycle. It pulses the optoisolator input current by discharging C_1 into the diode. Transistor Q1 is

switched off while the AD654 conducts. Q1 then recharges C_1 during the second half of the cycle.

The value of C_1 is chosen to suit the type of optocoupler. In practice, this value has been found to be less critical than the value of resistor required for conventional constant-current mode. Typical values range from 1 nF to 10 nF.

CIRCLE 522 PRBS GENERATOR SELF-STARTS

BRIAN BREWSTER

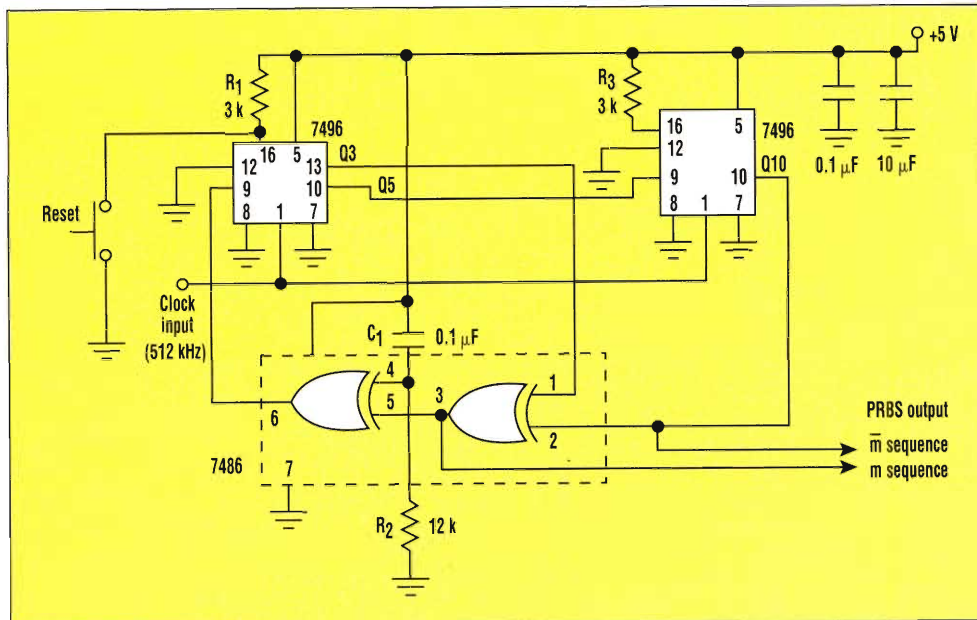
Satellite Microwave & Communications Ltd., Postbus 10416, 6000GK Weert, The Netherlands.

Pseudo-random bit sequences (PRBSs) are widely employed in various applications, such as test sources, noise generators, and scrambling and spread-spectrum systems. A common implementation is to employ an n-stage shift register with modulo-2 feedback at m taps to generate a maximum length sequence $2^n - 1$. These sequences will cycle through all n-bit states with the exception of the all-zero state. Therefore, at power initialization, the shift register will remain in a static condition, because $0 \oplus 0 = 0$, where \oplus denotes the exclusive-OR operator. As a result, additional logic is required to inject at least one logic 1 bit into the shift register at power startup.

In this circuit (see the figure), an additional exclusive-OR gate is con-

signal so that the PRBS generator can self-start at power-up. A shift-register length n of 10 is shown with feedback at stages 3 and 10, providing true and inverted maximal length sequence outputs.

This technique applies an input directly to the feedback loop. There-



ADDING AN EXCLUSIVE-OR GATE to a PRBS generator provides the generator with sufficient transient signal so that it can self-start at power-up.

nected after the modulo-2 feedback, with C_1 and R_2 applying the supply turn-on ramp into the feedback loop. This provides sufficient transient

fore, it's considered more reliable than applying an RC configuration to the shift-register reset input to create a random turn-on state. □

CIRCLE 523 GENERATING SINE WAVEFORMS

YONGPING XIA

EBT Inc., 2522 W. 237th St., Torrance, CA 90505.

A square waveform filtered by a high-order low-pass filter in which -3-dB frequency is lower than signal frequency will eliminate most harmonics of the waveform. As a result, the filter outputs a fundamental sine waveform. This method is applied to generate a sine waveform by using a switched-capacitor filter (MAX292) (see the figure). This circuit offers wide frequency range (0.1 Hz to 25 kHz), low distortion, and constant output amplitude in the whole fre-

quency range.

MAX292 (IC2) is an 8th-order low-pass Bessel filter. Its -3-dB corner frequency is determined by its clock frequency divided by 100. In other words, the corner frequency is 1 kHz if the clock 100 kHz. IC1 (74HC4060) is a 14-bit binary counter with a built-in oscillator. Its Q4 generates IC2's clock and Q10 sends a square waveform as IC2's input. Because the frequency ratio of the clock and input is 64:1 (which is lower than the -3-dB ratio), only the square waveform's

IDEAS FOR DESIGN

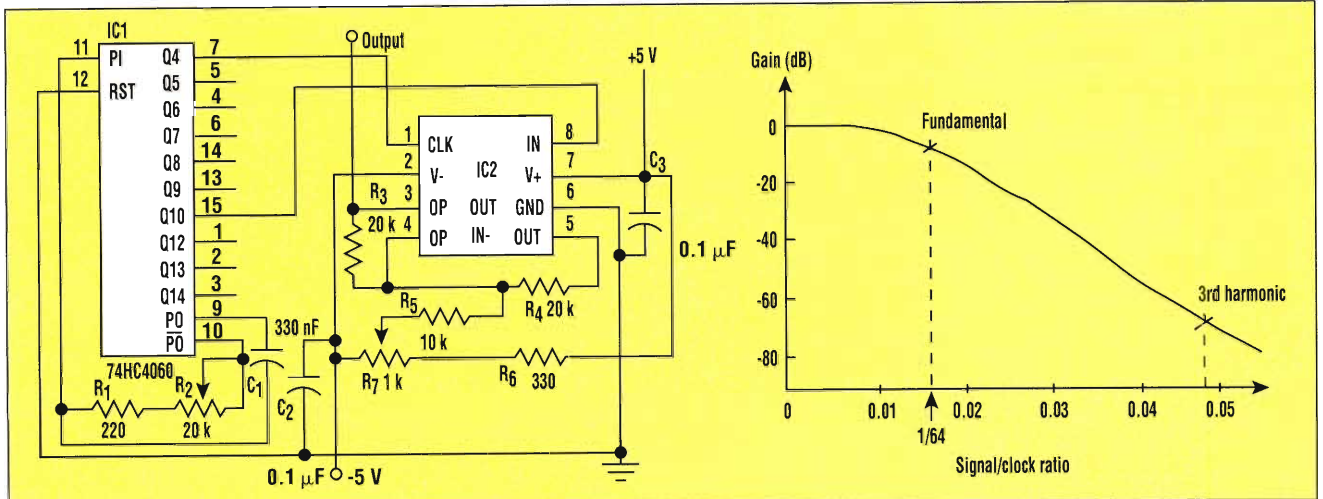
fundamental can partially pass through the filter, with about 9-dB loss. The third harmonic will be down about 65 dB.

Thus, the filter outputs a pure sine waveform with approximately a 2.5-V p-p amplitude. Because the ratio is

a constant, output amplitude will also be constant throughout the entire frequency range. IC2 contains an uncommitted op amp that's used to offset output dc level by adjusting resistor R_7 .

R_1 , R_2 , and C_1 determine IC1 oscil-

lation frequency, which is 16 times the output frequency. Useful output-frequency range is from 0.1 Hz to 25 kHz. By using the component values in the figure, it's possible to achieve a frequency range of 80 Hz to 7.5 kHz. □



A PURE SINE WAVEFORM can be generated with this circuit, which employs a switched-capacitor filter. Other key attributes are wide frequency range, low distortion, and constant output amplitude throughout the entire frequency range.

CIRCLE 521 SWITCHING BOOST REGULATOR USES 555

DAVID LAUDE

7040 Franciville Rd., Colorado Springs, CO 80908.

While working on a "B" battery replacement for antique battery-powered radios, it occurred to me that the venerable 555 timer might be able to handle most of a switching regulator's task. This circuit does just that (see the figure).

During operation, C_1 is alternately charged and discharged. Resistor R_1 ensures that C_1 begins charging. It also sets the minimum switching frequency. While C_1 is charging, pin 3 of the 555 timer drives Darlington pair Q1-Q2 to supply current to the inductor. When the inductor current reaches a value determined by R_2 and Q3's base-emitter turn-on voltage, the collector current of Q3 will rapidly charge C_1 .

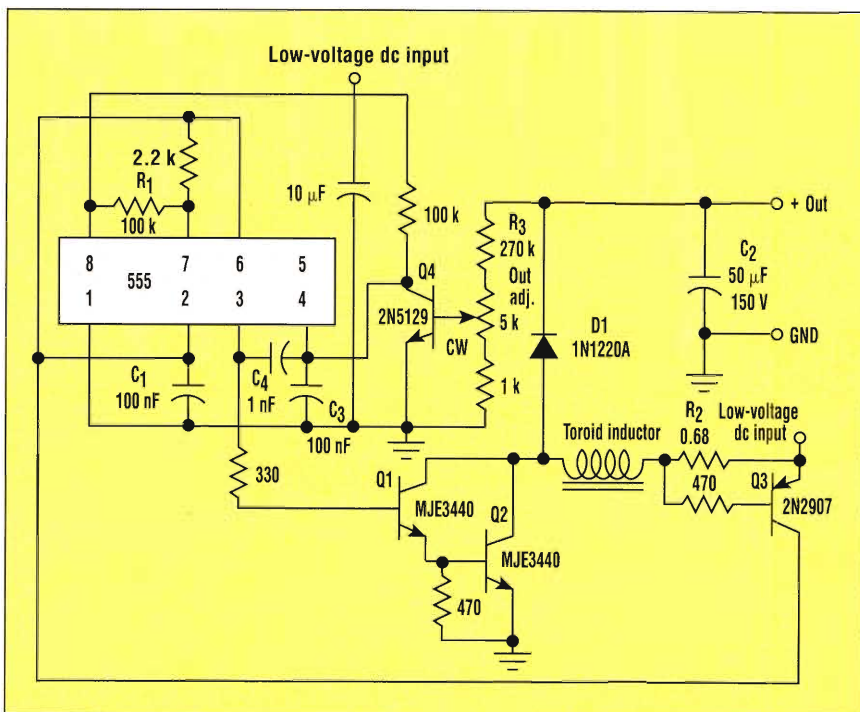
When the voltage across C_1 reaches the point where the 555 will reset, the voltage on pin 3 will go low, turning Q1-Q2 off. This action saves from consuming more power than is needed from the supply. At the same time, pin 7 will begin to discharge C_1 . During this turn-off event, the collector voltage of Q1-Q2 will be pulled high by the inductor's flyback action. Diode D1 steers the inductor current into storage capacitor C_2 . When C_1 's discharging voltage reaches the set threshold, pin 3 again goes high to repeat the cycle.

Output-voltage regulation is accomplished by monitoring the voltage across C_2 . Whenever Q4 turns on (an indication of excess output voltage) the collector pulls the 555's reset pin low. This turns off the drive to Q1-Q2 until the output voltage drops slightly. C_3 provides low-pass filtering to help the circuit remain stable during regulation. When pin 3 switches low, C_4 provides hysteresis to pin 4 for added stability.

The component values shown, chosen from my junk box, worked well to supply 80 V at 10 mA from a 7.5-V input with about 60% efficiency. The toroid's inductance is several hundred microhenries. R_3 can be modi-

control electronics will help to maximize performance. An additional capacitor, connected across pins 1 and 5 of the 555, will help reduce the influence of supply noise.

The circuit will exhibit some temperature drift due to the base-emit-



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CIRCLE 522 RUN OPTOISOLATOR AT 100 KHz, LOW POWER

B.R. BEER

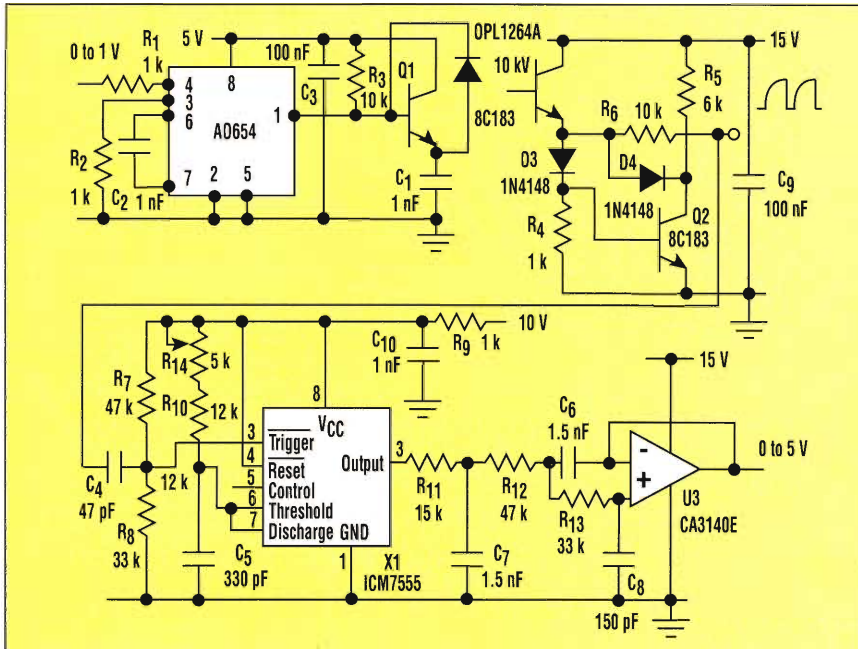
Fisons Instruments, Floats Rd., Wythenshawe, Manchester, United Kingdom M23 9LE.

This circuit can drive an inexpensive optocoupler with high voltage isolation at frequencies above 100 kHz using an AD654 voltage-to-frequency converter. The AD654 provides an open collector output with 50% conduction duty cycle. It pulses the optoisolator input current by discharging C_1 into the diode. Transistor Q1 is

switched off while the AD654 conducts. Q1 then recharges C_1 during the second half of the cycle.

The value of C_1 is chosen to suit the type of optocoupler. In practice, this value has been found to be less critical than the value of resistor required for conventional constant-current mode. Typical values range from 1 nF to 10 nF.

IDEAS FOR DESIGN



AN AD654 voltage-to-frequency converter is used to drive a high-voltage-isolation optocoupler at over 100 kHz. The converter, which supplies an open collector output with 50% conduction duty cycle, pulses the optoisolator by discharging C_1 into the diode.

If C_1 is too large, the phototransistor won't recover by the end of the cycle and Q_2 's collector voltage will remain low. For a transmission frequency of 100 kHz, an ideal value of C_1 will keep the collector voltage of Q_2 near to the ground rail for 5 μ s after the capacitor discharges. The circuit shown has operated at frequencies in excess of 180 kHz.

It's interesting to note that the response time from the discharge of C_1 to the falling edge of Q_2 is less than 200 ns. The average current taken by the optocoupler diode and drive transistor is proportional to frequency and is less than 1.5 mA at 100 kHz.

To complete the design, a CMOS 555 timer configured as a 5- μ s monostable followed by an active filter makes a low-cost frequency-to-voltage converter with a 0-to-5-V output range. Circuit nonlinearity is less than one bit for 8-bit applications. R_{14} is an offset control. \square

CIRCLE 523 KEEP I_C AND V_{CE} CONSTANT

S.J. PRASAD

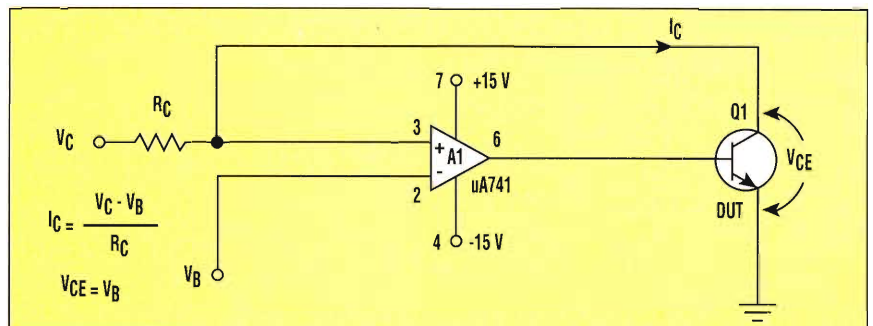
Tektronix Inc., Electronics Research Lab, P.O. Box 500, MS 50-223, Beaverton, OR 97077-0001.

Often, when making dc and rf measurements, it's necessary to bias a transistor at a precise collector current (I_C) and collector-emitter voltage (V_{CE}). In reliability tests, I_C and V_{CE} should be maintained constant even though the device's beta may be degrading with time.

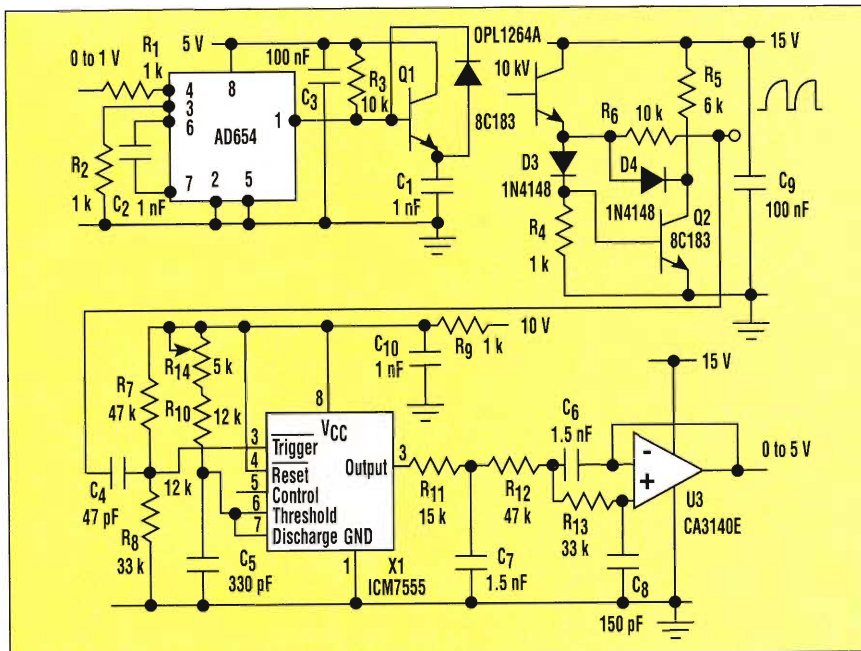
Conventional bias can't maintain

constant I_C and V_{CE} if there's a wide variation in beta (such as 5 to 500). Moreover, if the emitter must remain grounded for RF measurements, problems arise in maintaining a constant bias.

This circuit (*Fig. 1*) maintains constant I_C and V_{CE} . The device under test (DUT) is connected to op amp A1. The bias supply (V_B) is connected



1. BIASING A TRANSISTOR at a given I_C and V_{CE} is difficult if a wide variation exists in beta. Bias supply V_B sets V_{CE} . I_C can be set by V_C and R_C . However, I_C depends on V_B .



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CIRCLE 523 KEEP I_C AND V_{CE} CONSTANT

S.J. PRASAD

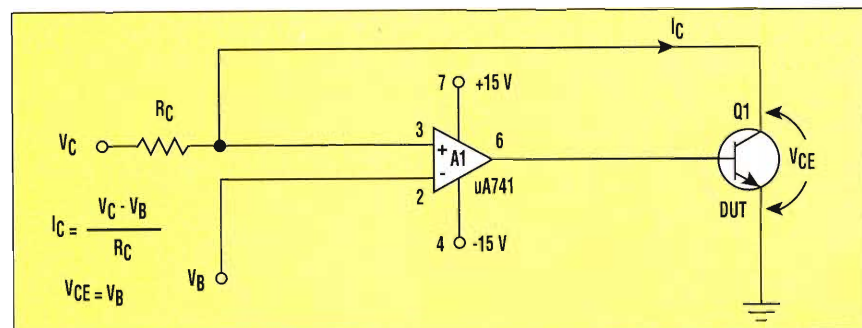
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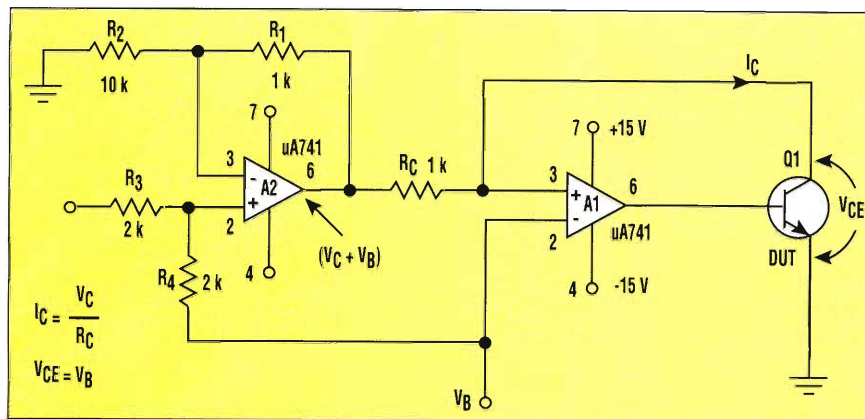
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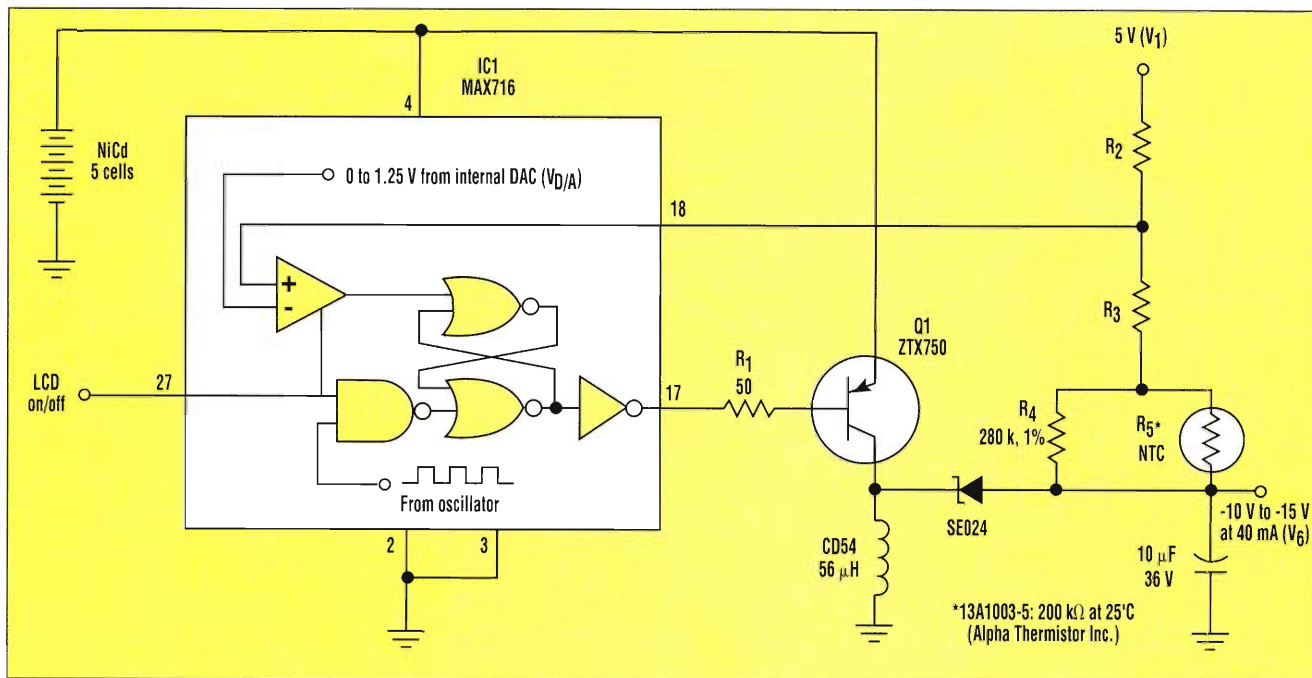


ure 1, it can be seen that I_C is now independent of V_B . Since I_C is now supplied by A2, V_C need not provide large currents. With $V_C = 1\text{ V}$ and $V_B = 5\text{ V}$, Q1 will be biased at $I_C = 1\text{ mA}$ and $V_{CE} = 5\text{ V}$. To prevent Q1 from oscillating, capacitors should be added at the collector and base terminals of the DUT. □

2. BY ADDING A NONINVERTING summing amplifier (A2) to the Figure 1 setup, I_C can be adjusted independent of V_B .

to the inverting input (pin 2) of A1. Because transistor Q1 is in the feedback loop with A1, the noninverting input (pin 3) is also at the same potential V_B . The noninverting input is connected to the DUT's collector, and V_B precisely sets V_{CE} . In addition, because the noninverting input doesn't draw any current, the I_C should come from the collector sup-

ply (V_C). By choosing V_C and R_C , the I_C be precisely set, independently of beta. However, if V_B is varied, I_C will change.
 To make I_C independent of V_B , a noninverting summing amplifier (A2) is added (Fig. 2). With the component values chosen, the output of A2 will always be at a potential of $V_C + V_B$. Comparing Figure 2 with Fig-



1. THE NEGATIVE TEMPERATURE-COEFFICIENT resistor R_5 modifies feedback in this switching regulator, which results in a negative output voltage that varies with temperature. With properly chosen resistor values, the circuit produces a temperature-compensated bias voltage that assures constant contrast in an LCD.

this setup, the circuit provides a linear bias change with temperature, from -10 V at 50°C to -15 V at -20°C (Fig. 2).

The automatic compensation is supplied by a negative-temperature coefficient resistor (R_5) that affects the feedback for the LCD-bias-voltage (V_6) regulator in IC1. Decreasing temperature, for example, causes an increase in R_5 's resistance and a consequent increase in the V_6 . R_4 linearizes the effect of R_5 , and R_3 adjusts the temperature coefficient of R_5 to that of the LCD (other temperature coefficients require different values for R_2 and R_3).

When calculating R_2 and R_3 , first note that V_6 is a function of $V_{D/A}$ and R_T . $V_{D/A}$ is the output of the internal 5-bit DAC, which enables the user to digitally adjust the LCD bias voltage. Also, R_T is the sum of R_3 and the parallel combination of R_4 and R_5 . In equation form, it's as follows:

$$V_6 = V_{D/A} - (5\text{ V} - V_{D/A})R_T/R_2$$

Therefore,

$$R_T = R_2(V_{D/A} - V_6)(5\text{ V} - V_{D/A})$$

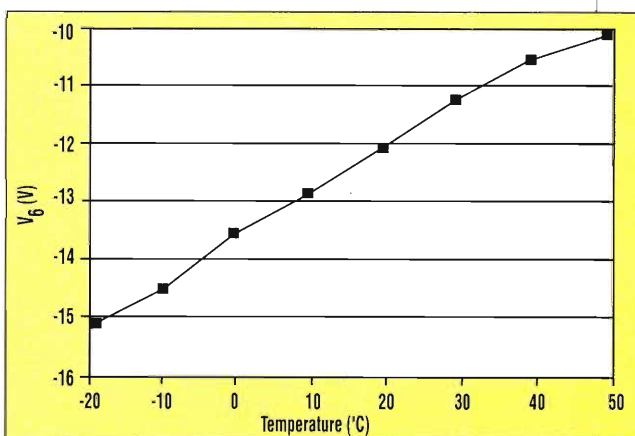
Solve for R_T at the extremes of V_6 (-10 V and -15 V) using the midrange value for $V_{D/A}$ (0.625 V): $V_6 = -10\text{ V}$, $R_T = 2.43R_2$; $V_6 = -15\text{ V}$, $R_T = 3.57R_2$.

Equivalent expressions for R_T are based on its definition: $V_6 = -10\text{ V}$, R_T

$$= R_3 + (R_5 @ 50^\circ\text{C}) || R_4;$$

$$V_6 = -15\text{ V}, R_T = R_3 + (R_5 @ -20^\circ\text{C}) || R_4.$$

From the R_5 data sheet, $R_4 = 277\text{ k}\Omega$ (choose $280\text{ k}\Omega$, 1%), $R_5 @ 50^\circ\text{C} = 52.7\text{ k}\Omega$, and $R_5 @ -20^\circ\text{C} = 250.1\text{ k}\Omega$. With that information, substitute those values in the previous equations, equate corresponding expressions for R_T , and solve for R_2 and R_3 . As a result, $R_2 = 172\text{ k}\Omega$ (use $169\text{ k}\Omega$, 1%); $R_3 = 365\text{ k}\Omega$ (use $365\text{ k}\Omega$, 1%). □



2. THE REGULATOR OUTPUT in Figure 1 serves as a temperature-compensated bias voltage for LCDs.

CIRCLE 523 PHOTODIODE-AMP NULLS AMBIENT LIGHT

R. MARK STITT and WALLY MEINEL

Burr-Brown Corp., 6730 S. Tucson Blvd., Tucson, AZ 85076.

Many applications use a photodiode to measure a light signal in the presence of ambient background light. Sometimes, the photodiode can be optically shielded from

background light to eliminate unwanted signals. Another solution is to use a photodiode-amplifier with a de-restoration circuit to reject low-frequency background light signals.

The circuit shown represents the

latter method (see the figure). It consists of a Burr-Brown OPT201 integrated photodiode and amplifier, and an external op amp for dc restoration. The OPT201 combines a large 0.090-by-0.090-in. photodiode and a high-performance transimpedance amplifier on one chip. This composite eliminates the problems common among discrete designs, including leakage current errors, noise pickup, and gain peaking due to stray capacitance. The dc-restoration circuit consists of a noninverting integrator driving the transimpedance-amplifier summing junction through a 100-k Ω resistor, R_3 . The current through R_3 cancels the current from the photodiode at signal frequencies below integrator's pole frequency to drive the output of the photodiode amplifier to 0 V. The pole frequency is set by R_2 and C_2 :

$$f_{-3\text{dB}} = (1\text{ M}\Omega) / (2\pi R_2 C_2 R_3)$$

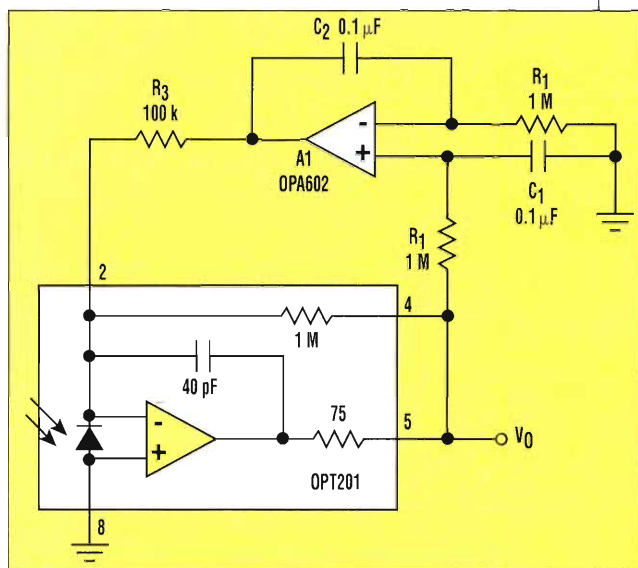
The 1-M Ω , 0.1- μ F values shown in the figure for R_2 and C_2 set the low-frequency cutoff pole at 16 Hz. Because of the long time constant, it may take more than one second for the circuit to come out of saturation when first powered up.

A noninverting integrator requires a matching pole. The matching pole, set by R_1 and C_1 , prevents photodiode-amplifier output signals above the pole frequency from feeding directly back into the summing junction of the transimpedance amplifier. Matching the poles isn't critical— $\pm 30\%$ tolerance is adequate for most applications.

The value used for R_3 depends on

the amplitude of the background light. With a 10-V output on A1, the 100-k resistor can provide a 100- μ A restoration current. This represents ten times the photodiode current that would otherwise drive the photodiode amplifier into saturation when using the internal 1-M Ω resistor. The dc-restoration circuit can remove a background signal many times larger than the ac signal of interest, thus supplying the increased signal-to-noise level critical in many applications.

Reducing the value of R_3 will increase the dc restoration range, but will also raise the noise gain of the transimpedance amplifier. Dropping R_3 to 10 k Ω would increase noise



A PHOTODIODE amplifier combined with a dc-restoration circuit will reject low-frequency ambient background light, easing measurement of a light signal.

from 130 μ V rms to 650 μ V rms. Values above 100 k Ω for R_3 will not substantially reduce noise. □

CIRCLE 522 FUSE SOUNDS OFF WHEN OVERLOADED

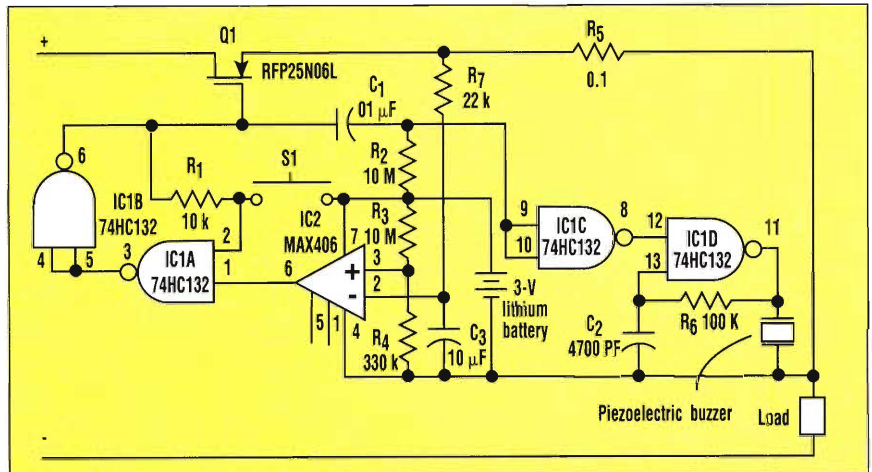
YONGPING XIA
EBT Inc., 23600 Telo Ave., Torrance, CA 90505.

Powered by a lithium battery, a self-powered solid-state fuse (see the figure) circuit that continuously measures the current running through it will cut off if the current is over 1 A, making a beeping sound for about 1 second. Because the circuit consumes only 1.2 μ A of current in normal condition, a 100-mAh battery can run at least eight years.

A logic-level FET (Q1) is used as an on/off switch. The current through Q1 has a little drop voltage on R_5 . This voltage compares with a constant voltage (0.1 V) provided by R_3 and R_4 . If the current is more than 1 A, IC2's output will change from high to low. This change triggers a flip-flop formed by IC1A, IC1B, and R_1 , so that IC1B's output becomes low. As a result, Q1 will turn off. High to low change on IC1B's output also generates a positive pulse (about 1 second) through C_1 , R_2 , and IC1C. This pulse allows IC1D, C_2 , and R_6 to oscillate, which in turns drives a buzzer. To reset the circuit, S1 should be pushed to the point where IC1B returns to output high status.

The circuit uses a minuscule current. During the period when there's no beep, total current is only about 1.2 μ A. Selecting a different R_5 or R_3R_4 ratio can change the fuse cur-

rent setting. The maximum working voltage depends on Q1, which is 50 V if a RFP25N06L FET is used. The RFP25N06L can handle transient current up to 25 A. The response time of the fuse depends on R_7 , C_3 , and overload current. □



WHEN LOAD CURRENT is over 1 a, this solid-state fuse will beep for about 1 second, signaling an overload. When the circuit isn't beeping, it uses very little current—about 1.2 μ A.

CIRCLE 523 ONE-TRANSISTOR DIFFERENTIAL AMP

DAVID L. ALBEAN

Thomson Consumer Electronics, Corporate Research Americas,
600 N. Sherman Dr., Indianapolis, IN 46201-2598.

A differential amplifier can be easily implemented with a one-transistor circuit, a combined common-emitter/common-base connection. (see the figure, a).

With the transistor biased at about 1 mA of collector current, gain expressions can be derived using superposition:

- The ac output voltage is of the form:

$$V_{out} = K_A V_A + K_B V_B$$

- The gain experienced by V_A is that of a common-emitter stage:

$$K_A = -R_3 / (R_4 || R_5)$$

- The gain experienced by V_B is that of a common-base stage:

$$K_B = +(R_3 / R_5)$$

Note that the gains are of opposite sign. By choosing the magnitudes of K_A and K_B to be equal:

$$V_{out} = K(V_B - V_A) \text{ where } K = (R_3 / R_5)$$

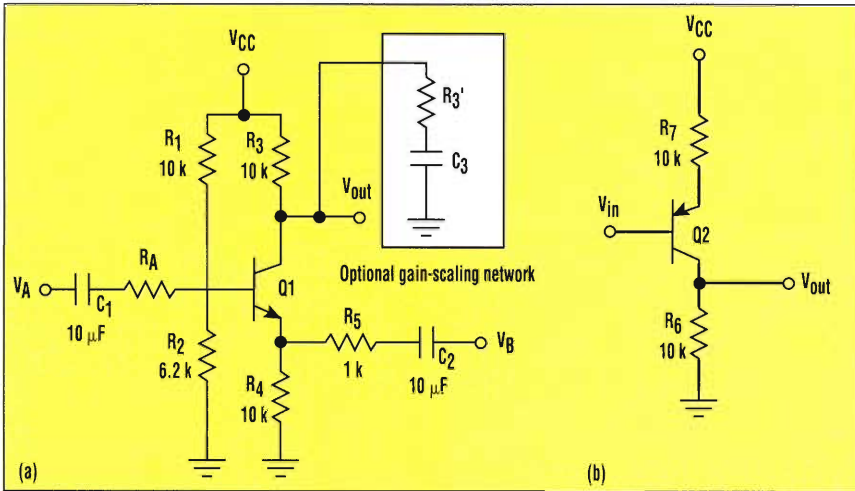
For K_A and K_B to be equal:

$$(R_4 || R_5) \approx R_5 \text{ (requires } R_4 \gg R_5)$$

It's evident that this circuit can implement $K_A \gg K_B$ by setting $R_4 \ll R_5$. For example, setting $K_A = 5$ and $K_B = 1$ allows easy realization of a function like $V_{out} = (V_B - 5V_A)$.

If very accurate subtraction is required, add resistor R_A as a gain trim for K_A . R_A will act as a voltage divider with the bias network ($R_4 || R_5$) to reduce the magnitude of value of K_A . This will allow K_A to be trimmed to match exactly the value of K_B .

Overall gain can be scaled via R_3 .



plication (see the figure, b). A pnp common emitter/common base circuit is employed.

The common-mode rejection of any ac ripple present on the V_{CC} line can be provided (due to imperfect bypassing), as long as the same ripple is present on its input (base). Again, the gains from the emitter and the base to the collector are equal but are opposite in sign.

The circuit probably is most useful in integrated circuit design, in which any remaining V_{CC} ripple can be cancelled by adding a stage of this type. □

THIS DIFFERENTIAL AMPLIFIER (a) uses only one transistor in a combined common emitter/common base connection. As a power-supply rejection circuit, a pnp transistor is used (b).

If a lower gain is required, a series R/C combination should be used in parallel with R_3 to reduce the gain.

Looking more closely at the figure, the component values implement $V_{out} = 10(V_B - V_A)$; C_1 and C_2 are

coupling capacitors; and R_1 and R_2 establish the dc bias and desired collector current. For $K = 1$, $V_{out} = (V_B - V_A)$, requires $R_3' = 1\text{ k}$.

This setup is also advantageous in a power-supply rejection circuit ap-

CIRCLE
521 STREAMLINE YOUR WIEN BRIDGE

ERIC KUSHNICK
LTX Corp., University Ave., Westwood, MA 02090.

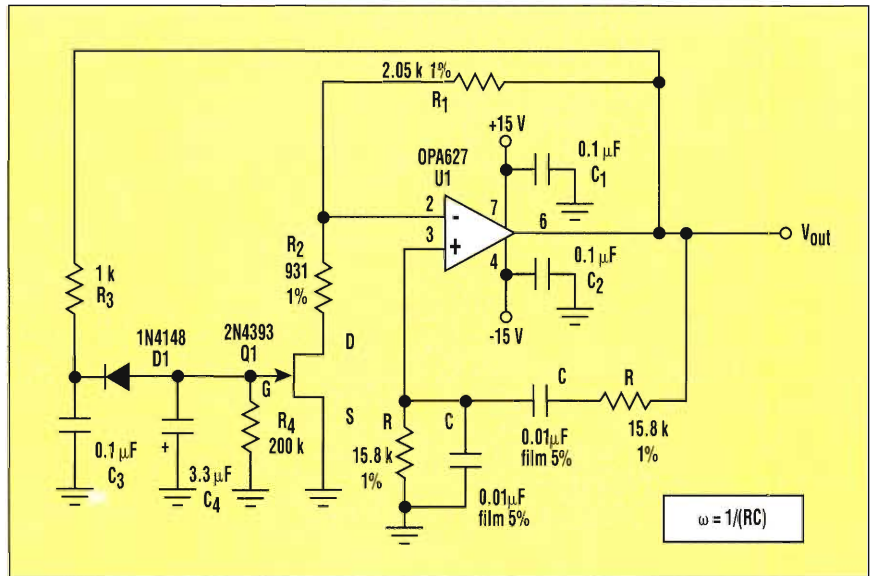
A Wien-bridge oscillator can produce a very low distortion sine wave at audio frequencies and beyond. It operates by carefully balancing a frequency-selective positive feedback with an equal amount of negative feedback around a high-gain amplifier. The amount of feedback must be continuously adjusted for proper operation. Some textbooks suggest a light bulb or a positive temperature-coefficient resistor for this purpose.

A FET can also do a nice job of controlling the feedback, but the ac voltage across the FET must be kept low to prevent nonlinearities from introducing distortion in the sine-wave output. The trick to overcoming these nonlinearities without sacrificing output amplitude is to use a resistor (R_2) in series with the FET (see the figure).

The two resistors (R) and two capacitors (C) comprise the frequency-selective positive feedback network, and set the frequency of oscillation: $f = 1/(2\pi RC)$. R_1 , R_2 , and the FET make up the negative feedback path. For the device to operate properly, R_1 must equal approximately $2 \times (R_2 + R_{FET})$, where R_{FET} is the effective resistance of the FET. R_2 must be small enough so that $R_2 + R_{FET}$ (minimum) is less the $1/2 \times R_1$, or the oscillator won't be able to start. The closer R_2 is to $1/2 \times R_1$, the less voltage will be dropped across the FET, and the lower the distortion at the oscillator's output.

The FET's gate threshold voltage controls the oscillator's output am-

plitude. R_4 and C_4 set the response of the gain control loop. The circuit given in the figure produces approximately 2.7 V p-p (about 1 V rms) of output at 1 kHz with a measured total harmonic distortion of better than -60 dB (0.1%). □



IN THIS WIEN-BRIDGE oscillator circuit, R_2 prevents FET nonlinearities from producing distortion in the output.

CIRCLE
522 DUAL V_{OUT} DAC TAKES LITTLE POWER

JOHN WETTROTH
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By using a combination of power-conserving tricks, a dual voltage-output DAC draws less than 20 μA from a 5-V supply (see the figure). The circuit suits a need for programmable voltage generation in slow or static applications, such as the nulling of offsets in a micropower instrument.

Current-output DACs typically waste power by routing the complement of I_{out} to ground. In this setup, that waste is avoided by operating each DAC in the reverse voltage-switching mode. The reference voltage is applied to the pins normally labeled I_{out} .

The I_{out} pins possess a constant and relatively low input impedance of 11 k Ω . To reduce input currents,

the reference voltage is scaled by 100 (from 5 V to 50 mV), and therefore delivers only 5 μA to each DAC input. Signal levels are restored by a compensating gain of 100 in each output amplifier. Inexpensive 10 M/100 k resistor networks are a good choice for the multiple 100:1 attenuators required. Though only 2% accurate, they offer much better capabilities in matching and tracking.

Greater scaling is impractical because of 0.5 mV (maximum) offsets in the output amplifier shown in the figure. Amplified by 100, these offsets produce worst-case output errors of $\pm 1\%$ (0.05 V). The errors are constant over temperature, but additional error due to drift over a range of 40°C is typically $\pm 1/2$ LSB. These

CIRCLE 521 BUILD IF/AGC AMP WITH FOUR PARTS

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An IF/AGC amplifier that features an 82-dB AGC range can be built using just four active components (see the figure). It uses a simple two-transistor peak detector (the transistors, 2N3904 and 2N3906, are commonly available and low cost).

The peak detector consists of Q2, a temperature-dependent current source, and Q1, a half-wave detector. Q2 is biased for a collector current of 300 μA at 27°C; the temperature coefficient is 1 $\mu\text{A}/^\circ\text{C}$.

The current into capacitor C_{AV} is the difference between the collector currents of Q2 and Q1, which is proportional to the output signal's amplitude. The automatic gain control voltage, V_{AGC} , is the time integral of the error current.

For V_{AGC} (and thus the gain) to remain insensitive to short-term ampli-

tude fluctuations in the output signal, the rectified current in Q1 must, on average, exactly balance the current in Q2. If the output of A2 is too small, V_{AGC} will increase. This in turn causes the gain to increase until Q1 conducts and the current through Q1 balances the current through Q2.

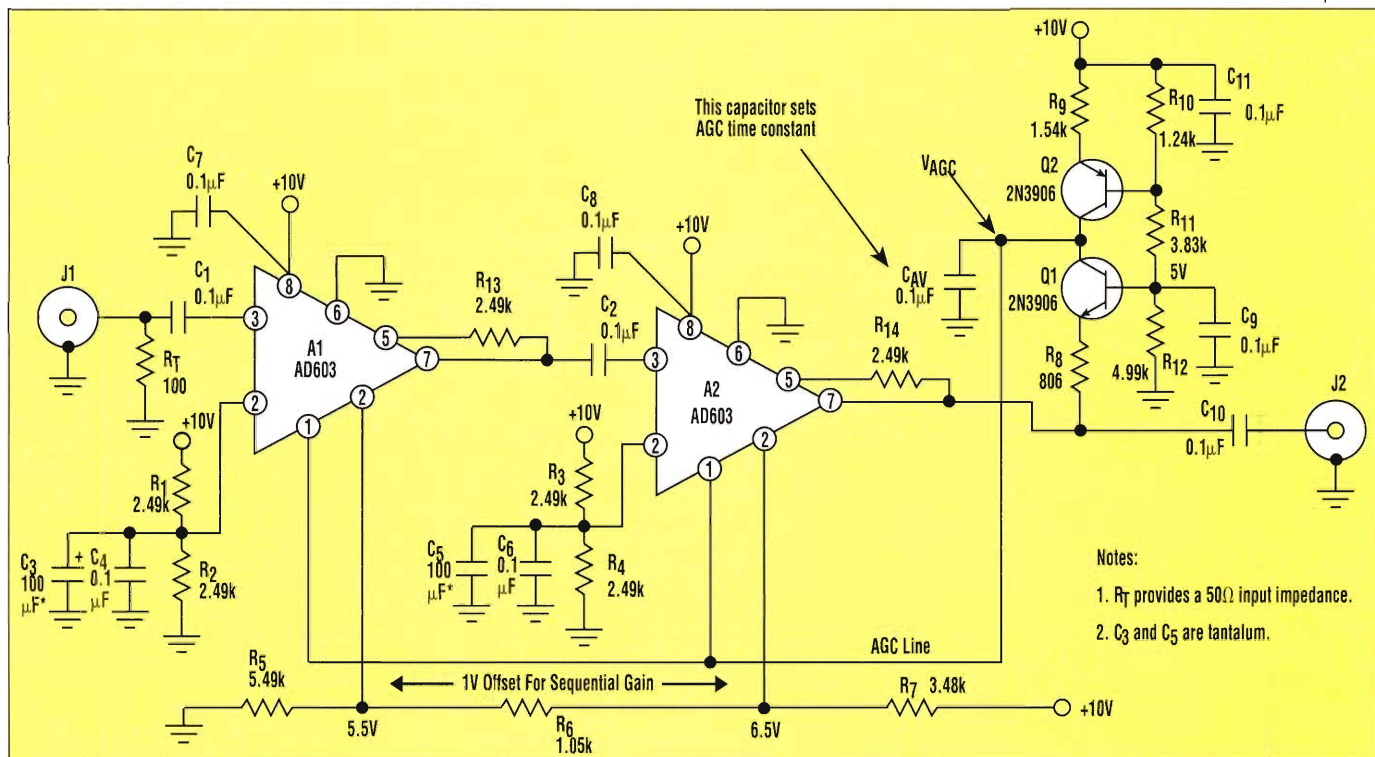
To illustrate further, first consider the case when R_g is zero and the output voltage V_{out} is a squarewave at, say, 455 kHz (which means it's well above the corner frequency of the control loop). During the time V_{out} is negative with respect to the base voltage of Q1, Q1 will conduct. When V_{out} is positive, Q1 cuts off. Because the average collector current of Q1 is forced to be 300 μA and the squarewave has a duty cycle of 1:1, Q1's collector current when conducting must be 600 μA .

Because Q1's average emitter cur-

rent is 600 μA during each half-cycle of the squarewave, a resistor of 833 Ω would add a PTAT (proportional to absolute temperature) voltage of 500 mV at 300 k, increasing by 1.66 mV/ $^\circ\text{C}$. In practice, the optimum value will depend on the type of transistor used, and to a lesser extent, on the waveform that optimizes the temperature stability. For the 2N3904/3906 pair and sinewave signals, the recommended value is 806 Ω .

The 1.8-kHz low-pass filter which R_g forms with C_2 reduces distortion due to ripple in V_{AGC} . The output amplitude under sinewave conditions will be higher than for a squarewave, since the average value of the current for an ideal rectifier would be 0.637 times as large. As a result, the output amplitude would be 1.88 (= 1.2/0.637) V, or 1.33 V rms. In practice, the somewhat non-ideal rectifier result in the sinewave output being regulated to about 1.4 V rms, or 3.6 V p-p.

The entire circuit operates from a single 10-V supply. Resistors R_1 , R_2 , R_3 , R_4 bias the common pins of A1 and A2 at 5 V. This pin is a low-impedance point and must have a low-impedance path to ground. In the cir-



- Notes:
1. R_7 provides a 50 Ω input impedance.
 2. C_3 and C_5 are tantalum.

JUST FOUR ACTIVE COMPONENTS are used in this configuration that provides 82 dB of AGC. Q1 and Q2 form a temperature-compensated peak detector that holds the output at 1.4 V rms for inputs as low as -67 dBm (100 μV rms) to +15 dBm (1.4 V rms).

cuit shown, it's provided by the 100- μ F tantalum capacitors and the 0.1- μ F ceramic capacitors.

The gain of A1 and A2 is set at 42 dB for an overall gain of 84 dB. They operate in sequential gain, which means that the gain of A1 goes from minimum to maximum and then A2's gain does the same. This is beneficial because first, the signal-to-noise ratio is at its maximum for as long as possible, and second, the signal strength in dBm can be determined from the AGC voltage (the gain changes at 40 dB/V). The gain is 0 dB for $V_{AGC} \approx 5$ V, and 82 dB for $V_{AGC} \approx 7$ V. In the circuit, the gain-control offset voltage between pins 2 (GNEG) of A1 and A2 is 1.05 V (42.14

dB \times 25 mV/dB), which is provided by a voltage divider consisting of R_5 , R_6 , and R_7 .

The circuit's bandwidth exceeds 40 MHz and can be used at any of the standard IFs (such as 455 kHz, 10.7 MHz, or 21.4 MHz) within this range. At 10.7 MHz, the AGC threshold is 100 μ V rms (-67 dBm) and its maximum gain is 83 dB ($20 \log 1.4 \text{ V}/100 \mu\text{V}$). The circuit holds its output at 1.4 V rms (3.9 V p-p) for inputs as low as -67 dBm to as high as +15 dBm (82 dB), where the input signal overdrives the amplifiers. For a -30 dBm input at 10.7 MHz, the second harmonic is 34 dB down from the fundamental and the third harmonic is 35 dB down. \square

CIRCLE 522 RMS CONVERTER HAS EXCELLENT CMR

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Designs for rms converters are common, particularly the single-chip monolithic solutions. This circuit (*see the figure*), however, differs from the others because of its versatile instrumentation-amplifier-type differential inputs that feature excellent common-mode rejection (CMR). In addition, the circuit is built with inexpensive, generic components.

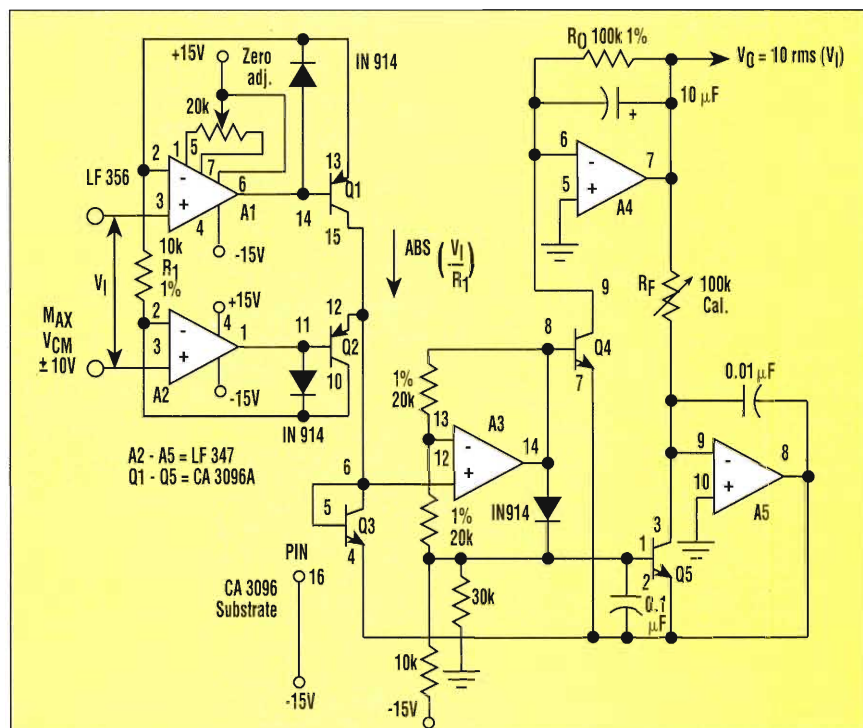
The first step in input-signal processing is the differential-input absolute-value circuit (ELECTRONIC DESIGN, April 16, 1992, p. 93). It consists of A1, A2, Q1, Q2, and input-scaling resistor R_1 . The zero-adjustment trimmer pot provided for A1 permits accurate calibration for low-level inputs. The absolute-value circuit displays a common-mode voltage range of ± 10 V, a CMR equal to that of A1 and A2, and an input impedance of $\approx 10^{12} \Omega$. It produces a current-mode output at the collectors of Q1 and Q2 with a magnitude of V_I/R_1 .

This current is applied to diode-connected Q3, which produces a voltage that's logarithmically related to $\text{abs}(V_I/R_1)$ as the first stage of signal processing in the rms computing cir-

cuit. The rms computation is performed by a variation of the so-called "implicit" method. The log signal

produced by Q3 is doubled by A3 and then applied to antilog transistor Q4. Because $\text{antilog}(2 \log(x)) = x^2$, the collector current of Q4 (I_{Q4}) is proportional to the instantaneous square of Q3's collector current. I_{Q4} is averaged and converted to output voltage V_O by A4.

Amplifier A5 and transistor Q5 produce a signal related to $\log(V_O)$, which is applied to the emitters of Q3



THIS RMS CONVERTER DIFFERS FROM other designs because it includes instrumentation-amplifier-type differential inputs. The inputs offer excellent common-mode rejection.

CIRCLE 520 COMBINATION FILTER ELIMINATES OP AMP

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The classic "state variable" two-integrator filter is known for its insensitivity to component variations, and its ability to provide three separate simultaneous outputs—low pass, high pass, and bandpass.

Typically, a quad op amp is used to implement the state-variable filter. The classic configuration employs two integrating amplifiers, a filter input amplifier, and a filter feedback amplifier.

The design described here combines both input and feedback amplifiers into one adder/subtractor amplifier, achieving a three-op-amp filter design (see amplifier UA in the figure).

The time constant $T_0 (= R_0 C_0)$ of integrators UB and UC should be at least five times smaller than $1/F$, where F is the filter's maximum bandwidth in hertz. The filter's gain and damping ratio are independently adjustable by resistors R_1 and R_3 .

The bandpass center frequency adjustment (resistor R_2) influences both the low-pass gain and damping characteristics. Feedback resistors

R and R' of amplifier UA can be arbitrarily and independently set between 5 k and 20 k Ω , typical.

R_1, R_2, R_3, R_4, R , and R' are preferably a monolithic resistor network. Because circuit action depends solely upon the ratios of these resistor values, the temperature tracking ratios would be nearly ideal in a monolithic network. The two R_0 resistors can also share the same monolithic network for maximum component density.

The accompanying box first lists the prototype equations for the filter circuit shown in the figure. The second part of the box lists the design equations for the example of a second-order Butterworth low-pass filter with a cutoff frequency of 100 Hz and a gain of 10.

The following steps would be taken when designing such a filter:

Using the equation:
 $H(s) = -3955150 / (395515 + 889s + s^2)$
choose a time constant as shown in the table:

$T_0 = 0.001$ sec. (i.e., $1/10$ of $1/F_c$).

PROTOTYPE AND DESIGN EQUATIONS FOR STATE VARIABLE FILTER

Filter Prototype Equations:

Characteristic equation:
 $D(s) = \omega_n^2 + 2\alpha\omega_n s + s^2$
where: ω_n = filter natural frequency in radians/s
 α = damping ratio
 s = complex frequency variable in radians/s

Low pass: $H(s) = \frac{-K_1 T_0^2}{D(s)}$ transfer function

$$\text{Gain} = \frac{K_1}{K_2}$$

Bandpass: $H(s) = \frac{K_1 T_0}{D(s)}$; Gain = $\frac{K_1}{K_3}$

Highpass: $H(s) = \frac{-K_1 s^2}{D(s)}$; Gain = K_1

Filter Design Equations:

$T_0 = R_0 C_0$ (integrator time constant in seconds)

$$K_2 = \omega_n^2 T_0^2$$

$$K_3 = 2\alpha \sqrt{K_2}$$

$$Q = 1/2\alpha \text{ (filter's } Q)$$

$K_3 = K_1 + K_2$ (provisional equation, see design example in text)

Then:

$$C_0 = 0.01 \mu\text{F}$$

$$R_0 = 100 \text{ k}\Omega$$

$$K_1 = T_0^2 3955150 = 3.960$$

$$\omega_n^2 = 395515$$

$$K_2 = \omega_n^2 T_0^2 = 0.396$$

$$\alpha = 889/2\omega_n = 0.707$$

$$K_3 = 2\alpha(K_2)^{1/2} = 0.890$$

Choose:

$$R = R' = 10 \text{ k}\Omega$$

Then:

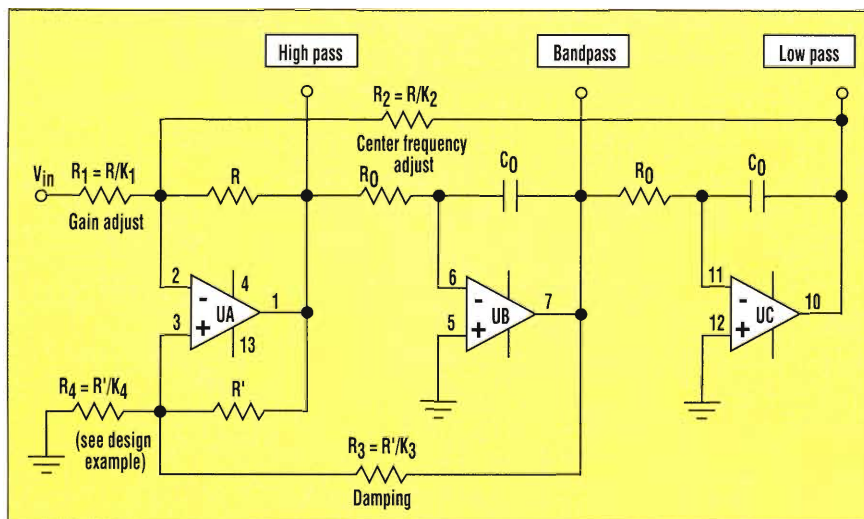
$$R_1 = R/K_1 = 2.52 \text{ k}\Omega$$

$$R_2 = R/K_2 = 25.25 \text{ k}\Omega$$

$$R_3 = R'/K_3 = 11.24 \text{ k}\Omega$$

The provisional equation in the design example portion of the table requires equality for amplifier UA. Because K_1, K_2 , and K_3 don't form a balance for the values calculated previously, K_4 must be added to the left side of the provisional equation to get that balance. This value is $K_4 = K_1 + K_2 - K_3 = 3.96 + 0.396 - 0.890 = 3.466$.

Next, set $R_4 = R'/K_4 = 10,000/3.466 = 2.89 \text{ k}\Omega$. Then connect R_4 to UA terminal 3. Should the reverse imbalance occur (although rare), find $K_4 = K_3 - (K_1 + K_2)$ and set $R_4 = R/K_4$. Finally, connect resistor R_4 to UA terminal 2. □



IN THIS THREE-OP-AMP 2nd-order state variable filter, the adder/subtractor amplifier (UA) drives two cascaded integrators (UB and UC). The two integrators' bandpass output is fed back to the adder terminal 3, and the low-pass output is fed back to the subtractor terminal 2. The high-pass output is formed at the adder/subtractor output.

CIRCLE 521 SINGLE-SUPPLY PHOTODIODE AMP

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good matching and temperature tracking at low cost when both packages come from the same manufacturing batch.

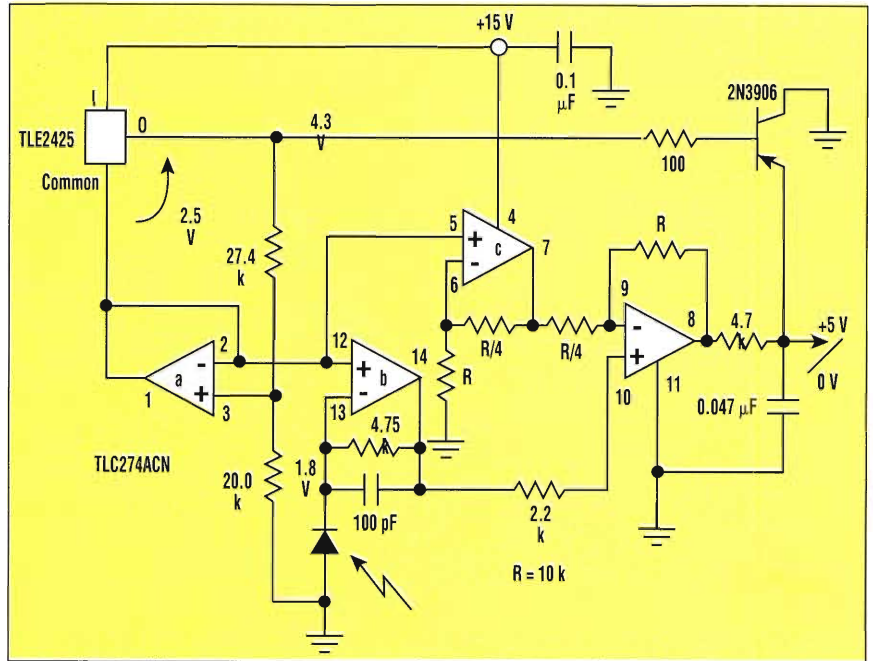
The photodiode is a Hamamatsu G1115, which is intended for use in the visible spectrum. □

This circuit offers many features that are commonly required in circuits using photodetectors (see the figure). For instance, it provides a reverse-bias operating point and output voltage offset, and uses a single-polarity power supply. On top of that, the circuit is designed to employ low-cost devices.

As shown in the schematic, the floating reference voltage from TLE2425 serves to bias the diode in a reverse-polarity mode. It also provides a clamping level at the output. Consequently, linear response to illumination is maintained for a 5-V range from dark current to full sunlight conditions.

Section b of the quad op amp is a current-to-voltage converter for photocurrent through the 4.75-k resistor. Bias voltage is fixed by the reference current (2.5 V/27.4 k) in the 20.0-k resistor.

Sections c and d of the quad op amp comprise a difference amplifier that has a gain that is set by the R, R/4 resistor pairs. These were chosen with pins 6 and 9 as the common node in a five-resistor SIP network. Four resistors can be paralleled simply by joining their terminals. The result is



THIS LOW-COST PHOTODIODE AMPLIFIER helps solve common problems associated with photodetectors, providing reverse bias operating point, output voltage offset, and a single polarity power supply.

CIRCLE 522 TWO REMOTE METERS USE ONE WIRE PAIR

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Driving two remote meters independently usually requires two wire pairs (one pair for each meter). However, this circuit drives two meters with only one wire pair, and its “constant current” design eliminates the effects of up to 200 Ω of wire-pair resistance (see the figure).

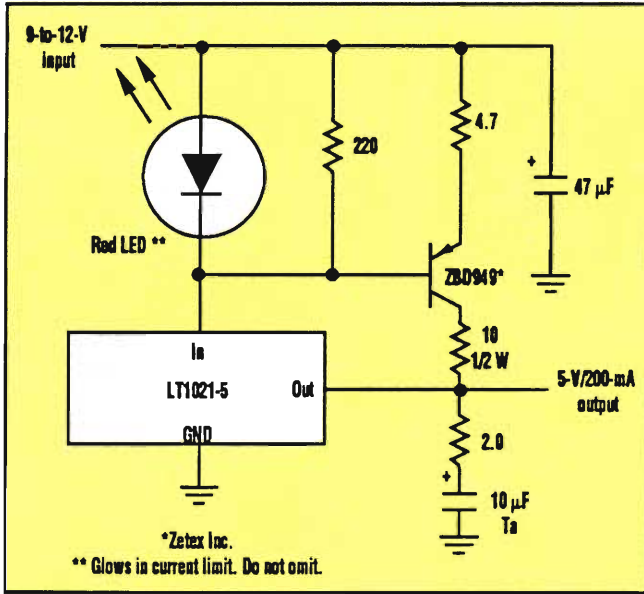
In the circuit, IC1 and IC2 generate a 40-Hz symmetrical square wave (the frequency isn’t critical). Q5 through Q8 amplify the square wave to 5 V p-p, which is applied to the “return” (black wire) for the remote meters.

Amplifier IC3A buffers the input

signal voltage V_{M1} , intended for meter M1 (0 to 8 V), and sends it through emitter-follower Q3 to a 100-Ω current-sense resistor. The other end of this resistor is tied to the “supply” (red wire) of the remote meters. IC3B amplifies the voltage across the sense resistor, which corresponds to the current sent to remote meter M1, and closes the feedback loop to IC3A.

This results in a voltage of 0 to 8 V at the M1 input, generating a current of 0 to 10 mA to M1. Transistor Q1 gates this current on and off synchronous to the 40-Hz square wave, so that meter M1 actually sees a 50%

IDEAS FOR DESIGN



USING this 5-V supply in place of a standard three-terminal regulator in a synthesizer oscillator lowers phase noise considerably. Output noise is just 7 μ V rms over a 10-Hz to 100-kHz bandwidth, and reference noise is guaranteed less than 11 μ V rms.

lasting the pass transistor and clamping the base drive. Although the oscillator only requires 200 mA, it's possible to extend the output current to at least 1 A by selecting an appropriate ballast resistor and addressing attendant thermal considerations in the pass transistor. \square

CIRCLE 523 FUNCTION GENERATOR IS STABLE, ACCURATE

MOSHE GERSTENHABER and MARK MURPHY

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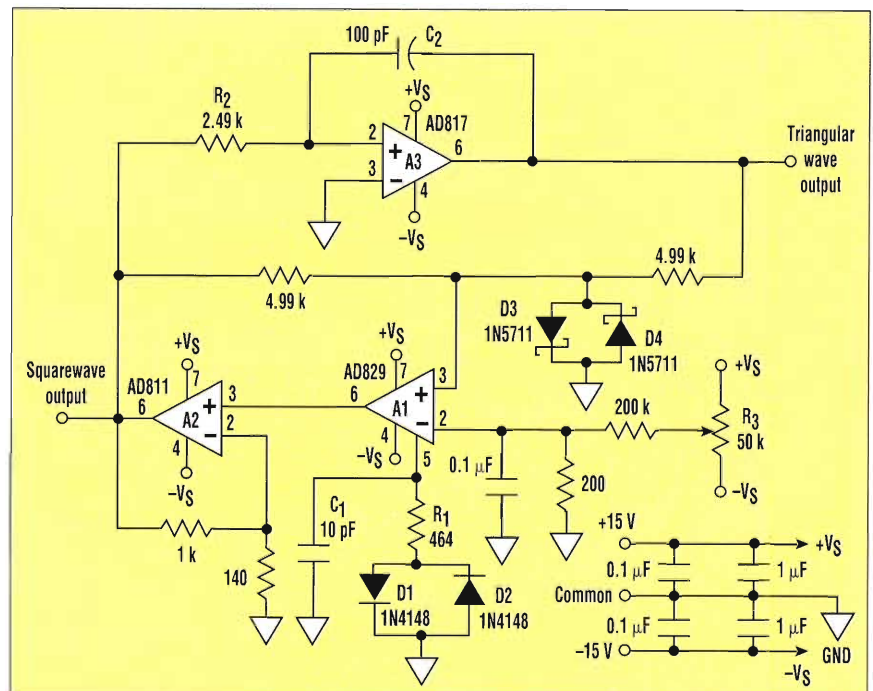
Virtually every electronics engineer knows how to design a circuit that will oscillate between the supply rails. However, those designs usually are sensitive to temperature and power-supply changes, are never symmetrical, and don't operate at high frequencies because the amplifier's output is saturated when it reaches the supply lines (thus taking added to unsaturate).

The circuit shown, a function generator, can alleviate these problems (Fig. 1). Its squarewave output boasts a rapid rise time, quick settling time, and an amplitude that's temperature insensitive. Also, its triangular output waveform features a perfectly constant rate of change throughout its range.

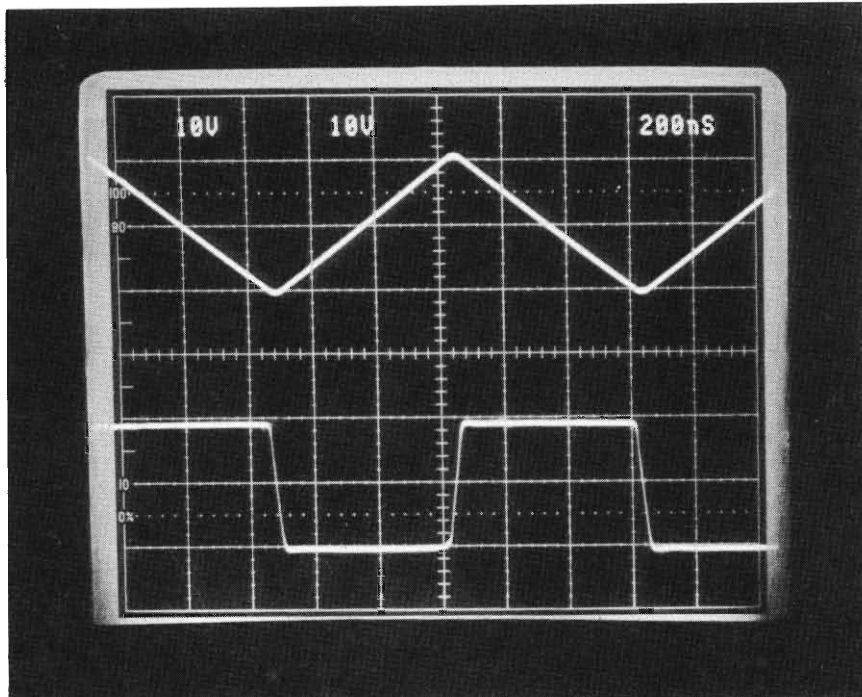
Looking at the schematic, amplifier A1 together with A2 generates a stable +10 V. This signal, which is integrated using A3, C_2 , and R_2 , makes a negative-going ramp. When the peak output of A3 equals -10 V, the output of A1 and A2 change state and the A3's output ramps up. When A3's output equals +10 V, the out-

puts of A1 and A2 change state again and a new cycle starts.

To control the amplitude of the squarewave (output of A2), A1's output is clamped using diode network D1 and D2 and resistor R_1 . This network also provides the amplitude stability of the oscillator. The current flowing into the high-impedance node of A1 is proportional to absolute temperature. When the correct value of the resistor is chosen (R_1), the approximately 2 mV/ $^{\circ}$ C decrease



1. THIS FUNCTION GENERATOR solves the problems typically associated with circuits designed to oscillate between the supply rails. Its square wave has a rapid rise and settling times, and an amplitude that's temperature insensitive.



2. THE UPPER TRACE of these output waveforms from the function generator represents the integrated waveform (the output of A3). The lower trace is the square wave (the output of A2).

in voltage drop of diodes D1 and D2 can be compensated for. As a result, the amplitude holds to its 1.2-V nominal value over the broad temperature range.

The Schottky diode network, D3 and D4, clamps and protects the input of A1. A2 operates in a noninverting configuration and amplifies the output of A1 to get 10 V. The frequency of oscillation is set by R_2 and C_2 , and is calculated using the equation:

$$f_o = 1/4R_2C_2$$

Capacitor C_1 limits the rise time of the squarewave and allows for a faster settling time. Potentiometer R_3 makes it possible to null the offset of the circuit.

Turning to the output waveforms of the oscillator (*Fig. 2*), the top trace is the integrated waveform (the output of amplifier A3) and the bottom trace is the squarewave (the output of amplifier A2). □

CIRCLE 520 LOCK DETECTOR NABS SINGLE CYCLE SKIPS

NORMAN R. COX

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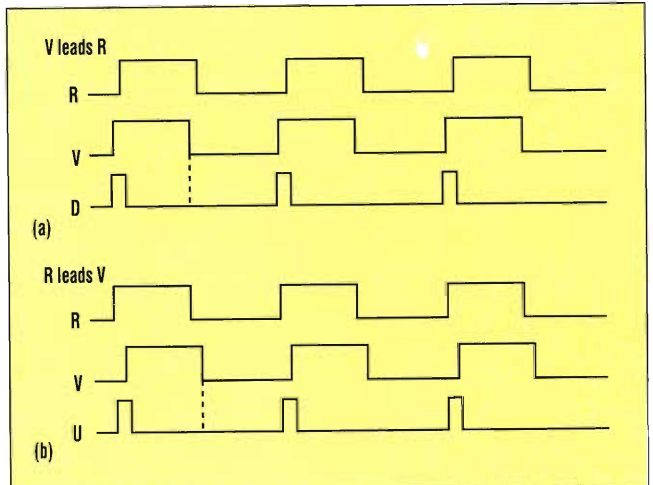
V signal is leading the input reference signal R (Fig. 2a), and the rising edge of R is suddenly lost, the D signal will remain HIGH throughout the interval. As a result, the flip-flop can be clocked HIGH. The flip-flop acts as a one-shot, causing the LED

A "lock" detector often is used with a phase-locked loop (PLL) or synthesizer to indicate when the loop is phase-locked with an input signal. Most of these detectors employ a simple phase detector (such as an exclusive-OR gate), a low-pass filter, and a threshold detector. These circuit can be helpful, but single cycle skips usually will go undetected due to the presence of the low-pass filter.

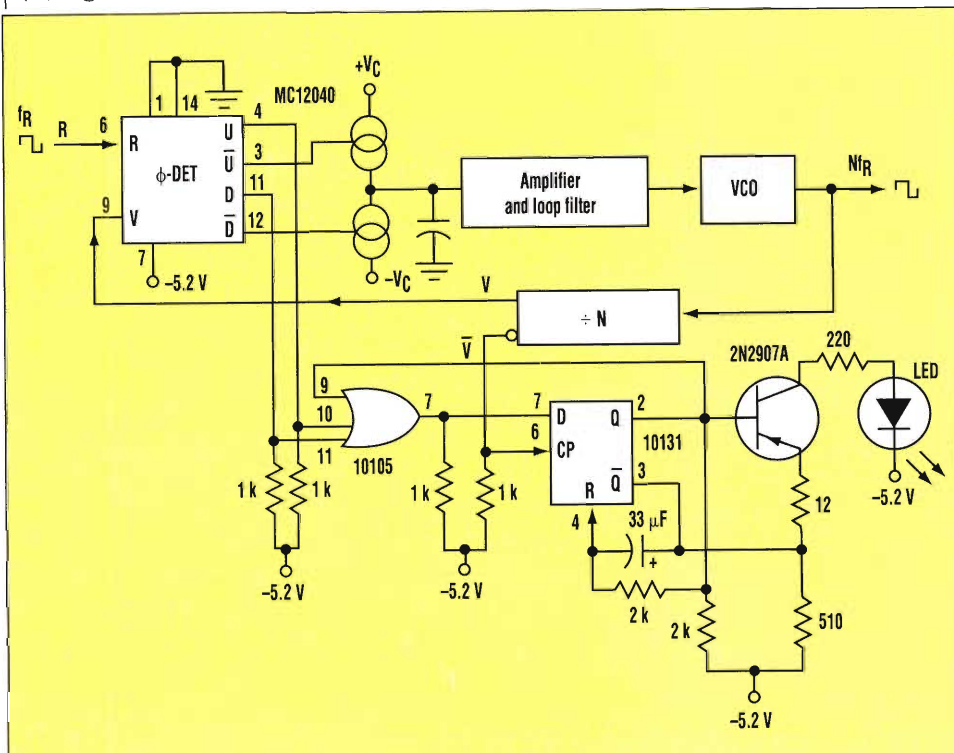
Using the method illustrated (Fig. 1) not only indicates the "locked" or "out-of-lock" condition, but also detects if even a single pulse or transition was missed. This knowledge becomes particularly useful in troubleshooting high-speed telecommunications systems that may derive reference signals from transmitted tones or carriers.

In the circuit, the Up (U) and Down (D) signals from the MC12040 ECL

phase detector are ORed with the output of a 10131 D-type flip-flop. When this signal is sampled by the flip-flop on the rising edge of the \bar{V} signal, the Q output should remain LOW when the loop is locked, because both the U and D pulses are very narrow (Fig. 2). The -0.8-V drop between Q and \bar{Q} keeps the transistor and LED turned ON, indicating the locked condition. If the



2. WHEN being sampled by the flip-flop, if the V signal leads the input reference signal R and the rising edge of R is lost, the D signal will remain HIGH throughout the interval, allowing the flip-flop to be clocked high (a). If the R signal leads the V signal when the transition is missed, the rising edge of the V signal will trigger the D signal of the phase detector, causing the LED to blink (b).



to blink OFF for about 0.1 seconds.

If the R signal is leading the V signal (Fig. 2b) when the transition is missed, the rising edge of the V signal will trigger the D signal of the phase detector, which will cause the LED to blink. If the loop isn't locked to the R signal at all, both the U and D signals will cause the one-shot to be continuously retriggered, and the LED will blink at a 5-Hz rate.

If it's suspected that missing transitions may be occurring, but with long periods of time in between, the connection to pin 4 of the flip-flop may be temporarily removed so that the circuit functions as a latch. The device is shown using ECL components, but the concept is directly applicable to TTL and CMOS circuits as well. □

1. THIS PLL LOCK INDICATOR not only can detect a "locked" or "out-of-lock" condition, but also even if a single pulse or transition has been missed.

CIRCLE 521 BUILD A TWO-PHASE RECTIFIER

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Many industrial applications require the measurement of rapidly changing single-phase ac signals as well as the conversion of these signals to a smooth dc level. One such example is measuring an ac current used to actuate a series of level detectors. However, because the ac signal is changing rapidly,

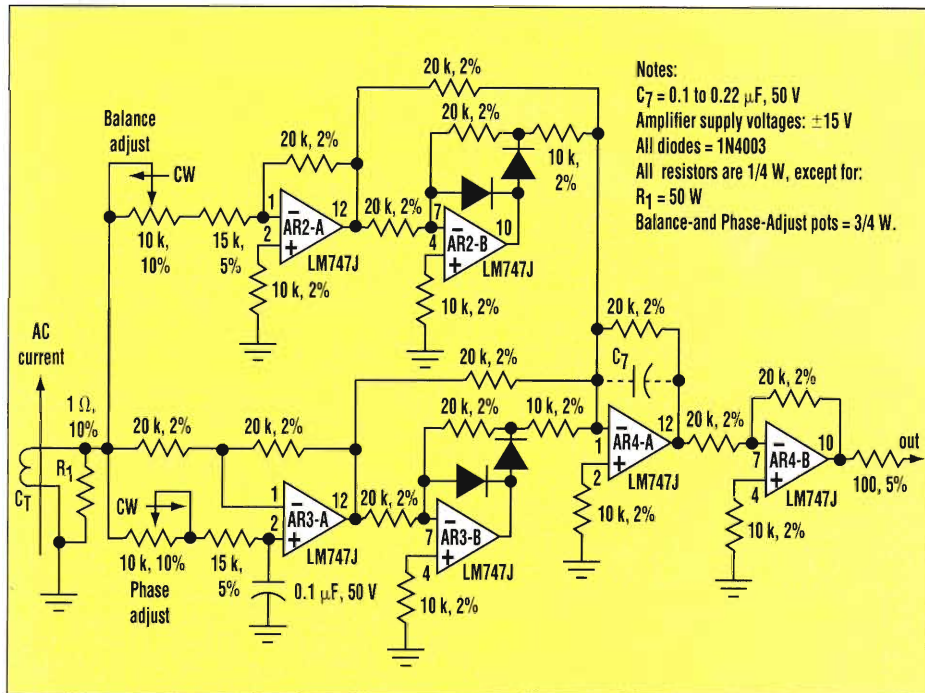
full-wave rectification and capacitor filtering isn't possible—response time would be too slow.

The circuit shown changes a single-phase ac signal to two phase, rectifies, and then sums the signal to a dc voltage level (Fig. 1). It can be seen by the waveform it generates (Fig. 2) that the ripple is less than half, and the ripple frequency is

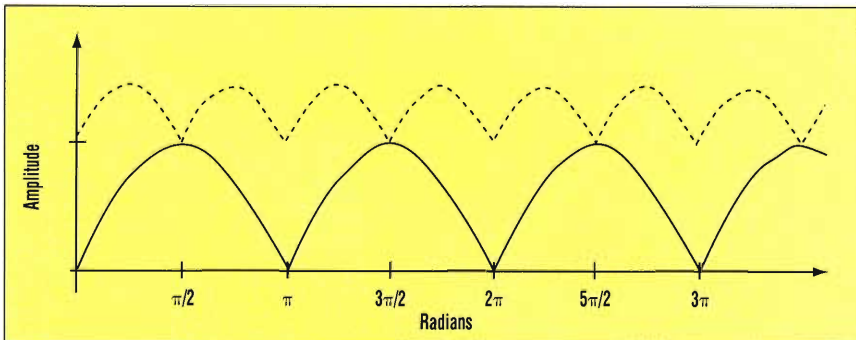
twice that, of the conventional single-phase circuit. Therefore, if some filtering is required, the capacitor may have a very small value. A filter capacitor may be connected across amplifier AR4-A (C₇) if desired.

Amplifier AR2-A measures the ac input signal. AR3-A also measures the ac input signal and phase-shifts it 90 electrical degrees. AR2-B and AR3-B rectify the two ac signals to dc levels. AR4-A sums the two dc current inputs, and AR4-B inverts the dc signal to a positive value. The dc output voltage is proportional to the ac input voltage generated across resistor R₁.

The circuit will follow amplitude changes in the ac input signal very rapidly, and works equally well with current or voltage inputs. □



1. A SINGLE-PHASE AC SIGNAL can be converted to two phase with this circuit. It rectifies and sums the signal to a dc voltage level.



2. THE WAVEFORM GENERATED by the two-phase rectifier illustrates that the ripple is less than half that of a conventional single-phase circuit's waveform. Also, the ripple frequency is double that of the conventional circuit.

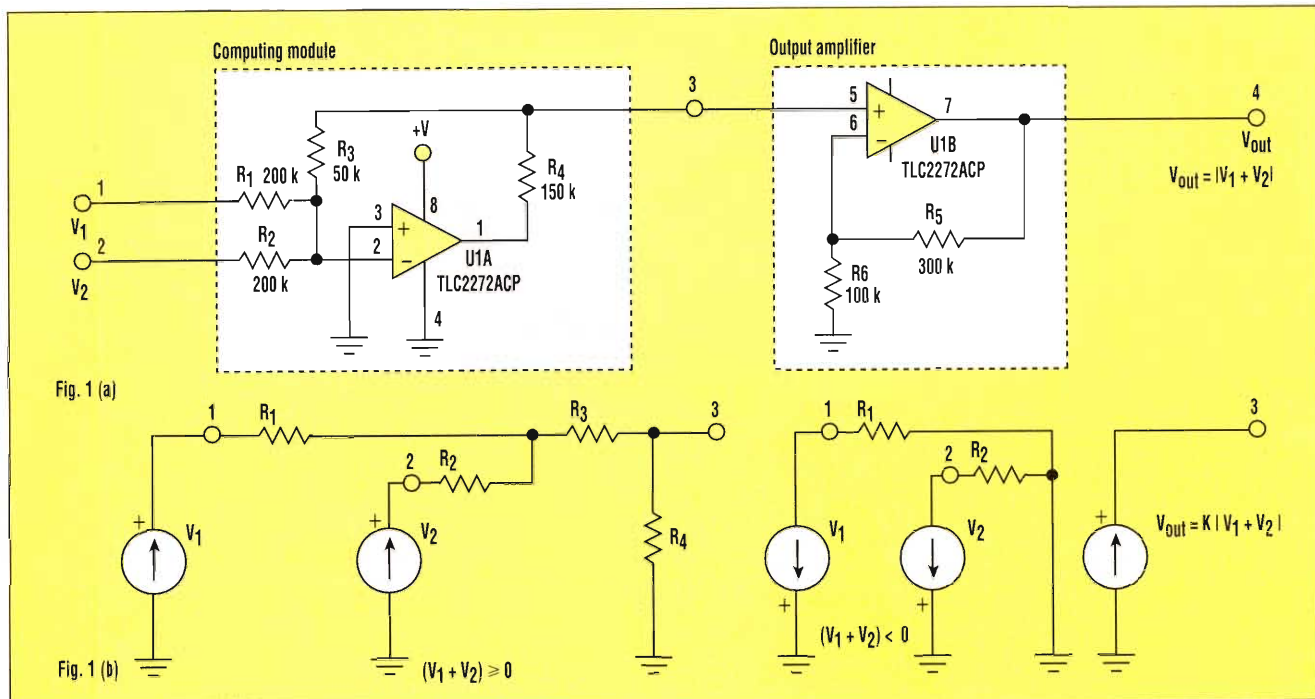


Fig. 1 (a)

Fig. 1 (b)

THE ABSOLUTE VALUE of the sum of the two input voltages is developed by the first stage of this circuit (a). The second-stage amplifier provides impedance matching and additional gain. The equivalent circuits (b) are used to analyze the overall circuit.

($R_1 = R_2 = r = R_3/K$), defines the main relationship between resistors R_1 to R_4 , needed to assure proper operation of the summing amplifier.

Note that if $K = 1/4$, the resistor ratio will be as shown in the figure, part a. If we define a basic resistance as R , then the relationships between the resistors are:

$$R_3 = R; R_1 = R_2 = 4R; R_4 = 3R.$$

It is important to note that the absolute values of the resistors do not matter; the values need only be "ratio-matched." Thus, any standard low-cost resistive network will be applicable.

The output terminal 3 may be connected directly to a digital multimeter or analog-to-digital converter with high input impedance. For better impedance matching, the additional noninverting output amplifier is recommended.

The optional amplifier provides impedance matching and produces an additional gain of $(1 + R_5/R_6)$. If R_5 is set equal to $3R_6$, unity gain of the whole amplifier is obtained. Consequently, the circuit returns the absolute value of the sum $|V_1 + V_2|$ of the input voltages.

However, all practical op amps in-

roduce errors. In this application, the most critical dc error source is the parasitic positive voltage on pin 1 of op amp U1A when $V_1 + V_2 > 0$. In an ac mode, the input capacitance of U1 defines the frequency bandwidth.

When the values of resistors are as is shown (see the figure, a, again),

the frequency range measured at the -3-dB points spans from dc to 20 kHz. To obtain a wider frequency range, lower resistances for R_1 to R_4 must be used. Also be aware of the possible nonlinear distortion, which could result from variations in the input capacitance of op amp U1 with changes in input voltage. □

CIRCLE 523 SIMULATE FERRITE LOSSES WITH CURVES

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The increasing number of applications involving soft-ferrite components can be attributed to the higher frequencies employed in today's switching power-supply systems. Higher frequencies are desirable because the higher the frequency, the smaller the transformer and the other wound components requiring a soft-ferrite core.

The choice of ferrite core thus is critical to shrinking the size of the power supply. Today's power supplies work at frequencies from 70 to

300 kHz, and sometimes range up to 1 MHz, with magnetic flux density up to 4000 to 5000 Gauss.

The choice of ferrite core also is critical to the reliability of the power supply. If the ferrite core isn't carefully dimensioned, the temperature rise due to power losses can reach as high as 40°C.

Moreover, the whole assembly might be in an environment that's at 50° to 60°C in its worst-case condition. As a result, that ferrite will saturate further and approach the "run-away" point (see "b1" in the figure),

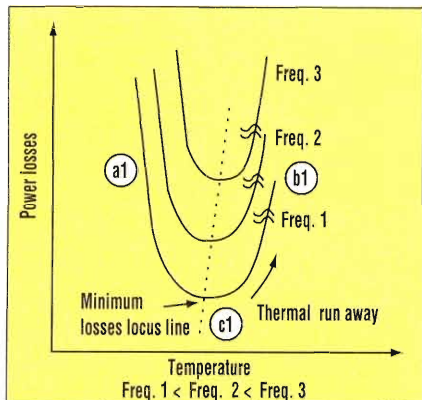

```

10 CLS:SCREEN 9:COLOR 15,1:KEY OFF
20 REM TO TEST PROGRAM REMOVE 'REM' FROM LINE 30 & LINE 40 !!
30 REM T1=25:T2=35:T12=15:T22=20:B1=100:B2=350:P22=120
40 REM F1=50:F2=300:P3=150:P1=50:P12=76:P2=90:GOTO 320
50 REM -----WARNING-----
60 REM In case program doesn't work well please check you inputted DATA !!
70 REM -----END WARNING-----
80 PRINT "General curve of Power Losses is: y = f( B, T, F )"
90 PRINT "< B is Magnetic Flux Density, T core temperature, F work frequency >"
100 PRINT "-----"
110 PRINT
120 PRINT "Symbols: 'cl' -> minimum loss point, 'a1' -> a point at the left of 'cl'"
130 PRINT
140 INPUT "1 [B magnetic Flux density of curve: mT]:";B1
150 INPUT " [T of point 'cl': C]:";T1
160 INPUT " [PW power loss of 'cl': mW/cm]:";P1
170 INPUT " [T of point 'a1': C]:";T12
180 INPUT " [PW power loss of 'a1': mW/cm]:";P12
190 INPUT " [F work frequency of the curve: kHz]:";F1
200 PRINT "-----"
210 PRINT "Take another curve with same B as curve 1, different frequency and"
220 PRINT "read Data for the point 'cl' ( minimum loss point of chosen curve."
230 INPUT " [F New work frequency of the curve: kHz]:";F2
240 INPUT " [PW power loss of 'cl' for new frequency: mW/cm]:";P3
250 PRINT "-----"
260 PRINT
270 INPUT "CURVE 2 [B magnetic Flux density of curve: mT]:";B2
280 INPUT " [T of point 'cl': C]:";T2
290 INPUT " [PW power loss of 'cl': mW/cm]:";P2
300 INPUT " [T of point 'a1': C]:";T22
310 INPUT " [PW power loss of 'a1': mW/cm]:";P22
320 REM ***** CALCULUS SUBROUTINES *****
330 ON ERROR GOTO 1320
340 COB1=P1:COB2=P2:DX1=T1:DX2=T2:PL0=P2
350 COA=(P12-P1)/(T12-T1)^2:COA2=(P22-P2)/(T22-T2)^2
360 ESPA=1:ESPB=1:ESPF=1:ESFF=1
370 A=COA*(B2/B1)^ESPA:ESPA=(COA2-A)^-1+ESPA
380 IF ABS(COA2-A)/COA2<0.01 THEN GOTO 400
390 GOTO 370
400 B=COB1*(B2/B1)^ESPB:ESPB=(COB2-B)^-0.001+ESPB
410 IF ABS(COB2-B)/COB2<0.01 THEN GOTO 430
420 GOTO 400
430 DX=DX1*(B2/B1)^ESPX:ESPX=(DX2-DX)^-0.001+ESPX
440 IF ABS(DX2-DX)/DX<0.01 THEN GOTO 460
450 GOTO 430
460 PLX=PL0*(F2/F1)^ESPF:ESPF=(P3-PLX)^-0.001+ESPF
470 IF ABS(PLX-P3)/PLX<0.01 THEN GOTO 490
480 GOTO 460
490 PRINT "-----"
500 INPUT "-----END CALCULUS-> ENTER-----";R1S
510 CLS:PRINT "The Modulation curve for your FERRITE core is solved."
520 PRINT "-----"
530 PRINT
540 PRINT "EQUATION SOLVED: ";PRINT
550 PRINT ">>> PL=( ";INT(COA*100)/1000;"*(Bwork/";B1;" )^";
560 PRINT " ";INT(ESPA*100)/100;"*(TEMP-";T1;" )^";
570 PRINT " *(Bwork/";B1;" )^";INT(ESPF*1000)/1000;"*";
580 PRINT " *(INT(1000*COB1)/1000;"*(Bwork/";B1;" )^";INT(ESPB*100)/100;" )";
590 PRINT " (Freq/";F1*1000;" )^";INT(ESFF*100)/100
600 PRINT
610 PRINT "-----"
620 INPUT "Calculate Losses (Y/N):";R1S
630 IF R1S="N" GOTO 1360
640 IF R1S="Y" GOTO 660
650 GOTO 620
660 CLS
670 PRINT "-----"
680 PRINT "YOU ARE ASKING FOR POWER LOSSES IN FERRITE."
690 PRINT "-----"
700 PRINT
710 INPUT "(F)requency work (kHz):";FREQ:FREQ=FREQ*1000
720 INPUT "(T)emperature of core (C):";TEMP
730 INPUT "(B) level max (mT) ";BLAVORO
740 INPUT "(I) interval between B curves (mT)";INTB: IF INTB=0 THEN 740
750 INPUT "(II) interval between Temperature calculus (C)";INTT
760 IF INTT=0 THEN 750
770 PRINT "-----"
780 PRINT "Pulse shape parameter: ";
790 PRINT "-----"
800 PRINT "1-sinus wave [enter 1]";
810 PRINT "2-square pulse [enter 2]";
820 PRINT "3-square bipolar [enter 3]";
830 INPUT "Pulse shape (1,2,3)";R1:R1=ABS(R1)
840 IF R1<1 OR R1>3 THEN 830
850 ON R1 GOTO 860,870,880
860 FORMA=1:GOTO 890
870 INPUT "Give a parameter between : 0.7-0.8";FORMA:GOTO 890
880 INPUT "Give a parameter between : 1.8-2.2";FORMA:GOTO 890
890 INPUT "Max PL on plot (max. mW/cm)";SCALEY:IF SCALEY <=0 THEN 890
900 CLS:PRINT "-----RESULTS OF CALCULATION-----"
910 LOCATE 3,50:PRINT "Losses in mW/cm3 ";
920 LOCATE 4,50:PRINT "Curves every 10 mT ";
930 LOCATE 22,1:PRINT " [ 75 ] 150 C "
940 LINE(10,20)-(390,290),12,B:FOR TIME=1 TO 10
950 LINE(10+TIME*38,20)-(10+TIME*38,290),10
960 LINE(10,20+TIME*27)-(390,20+TIME*27),12:NEXT TIME
970 LOCATE 3,15:PRINT " Max PL (mW/cm3)";SCALEY;" "
980 INIMAX=BLAVORO
990 GOSUB 1010
1000 GOTO 1060
1010 PL=COA1*(BLAVORO/B1)^ESPA*(TEMP-DX1*(BLAVORO/B1)^ESPX)^2
1020 PL=PL+COB1*(BLAVORO/B1)^ESPB
1030 PL=PL*(FREQ/F1/1000)^ESPF
1040 PL=PL*FORMA
1050 RETURN
1060 LOCATE 6,50:COLOR 13:PRINT "Your work condition: ---"
1070 LOCATE 7,50:PRINT "B level (mT)";BLAVORO
1080 LOCATE 8,50:PRINT "PL ";INT(10*PL)/10
1090 COLOR 11:LOCATE 7,50:PRINT "PL (mW/cm3)";INT(10*PL)/10;" "
1100 LOCATE 23,1:PRINT " PAUSE to HALT PLOT !> <Enter to prosecute...>"
1110 FOR BLAVORO=1 TO 500 STEP INTB
1120 FOR TIME=1 TO 150 STEP INTT
1130 GOSUB 1010
1140 LOCATE 10,LOCATE 8,50:PRINT "PL CURVE (mW/cm3)";INT(10*PL)/10;" "
1150 CLR = 14: IF PL<0 THEN PL=0:GOTO 1210
1160 IF BLAVORO>9*INIMAX AND BLAVORO <1.1*INIMAX THEN CLR=13
1170 IF PL<300/SCALEY < 290 AND TEMP<1 THEN 1190
1180 GOTO 1210
1190 TY=270/SCALEY*PL:TX=380/150*TEMP
1200 LINE(10+TX,290-TY)-(10+380/150*TEMP,1,290-270/SCALEY*PL),CLR
1210 TEMP1=TEMP:PL1=PL
1220 NEXT TEMP
1230 NEXT BLAVORO
1240 LOCATE 3,15:PRINT " Max PL (mW/cm3)";SCALEY;" "
1250 LOCATE 23,1:PRINT
1260 LOCATE 23,1:INPUT "New calculus (Y/N)";R1S:IF R1S="N" THEN 1290
1270 IF R1S="Y" THEN 660
1280 GOTO 1260
1290 LOCATE 23,1:INPUT "End calculus (Y/N)";R1S:IF R1S="N" THEN 1260
1300 IF R1S="Y" THEN 1360
1310 GOTO 1290
1320 REM --- ERROR SUB. ---
1330 COLOR 12
1340 INPUT " ONE DATA OR MORE IS ERRONEOUS, PLEASE CHECK..enter >";R1S
1350 RESUME 10
1360 CLS:END

```

which will cause the power supply to fail.

To limit the core temperature below 35°C, it's necessary to know the ferrite's power-loss characteristics, which are reported in its data sheets.



THE CURVES illustrate a ferrite core's power losses versus temperature (T) and frequency (F). If not carefully dimensioned, the ferrite will saturate and approach the "run away" point (b1), causing the power supply to fail.

The typical situation is that only a few curves are included, and consequently, interpolation is required. The interpolation would be easy if the power losses depended on one or two parameters, either temperature (T), magnetic flux density (B), or frequency (f). Unfortunately, that's not the case, and all three parameters must be interpolated together.

The program listing, shown above, was compiled specifically for modeling the ferrite losses over the f, T, and B parameters. The programming language is Basic because many computers support it. The program calculates the curves, first feeding the losses at two f, T, and B conditions by interpolation and then with a successive-approximations process.

The curves work very well in the manufacturer's defined field of ferrite application as reported in the data sheet. Outside these limits, the results should be modified with a figure of confidence. □

IFD WINNERS

Winner for August 8, 1994

Johnnie Molina, Burr-Brown Corporation, Tucson, AZ 85706; (602) 746-7592. His idea: "Programmable Analog Filter."

Winner for August 22, 1994

Frank N. Vitaljic, 514 13th Street, Bellingham, WA 98225. His idea: "Convert To Digital Filters With Ease."

Winner for September 5, 1994

M.J. Salvati, Flushing Communications, 150-46 35th Avenue, Flushing, NY 11354; (718) 358-0932. His idea: "Add A Diff Amp To Your Scope."

Winner for September 19, 1994

George Altemose, Pall Instrumentation Technology, 95 Oser Avenue, Hauppauge, NY 11788; (516) 273-0911. His idea: "Very Efficient Solenoid Driver."

CIRCLE 520 STATE VARIABLE FILTER IS VERSATILE

HAORAN HE

Quantum Corp., 333 South St., SHR 1-3/E26, Shrewsbury, MA 01545.

The state variable filter shown (see the figure), which consists of only three op amps and a few passive components, provides several key features. These include the ability to simultaneously provide low-pass, high-pass, and bandpass filter functions, and adjust bandwidth in a wide range by changing the values of C_f and R_f . The device also is easy to tune and simple to construct, while the quality factor Q of each filter is independent of each other.

Two input modes are employed. For the low-pass and high-pass filters, the inverting input is used while leaving the noninverting input open. The filters' cutoff frequency, gain, and quality factor are:

$$\omega_c = 1/(C_f R_f)$$

$$A = R/R_g$$

$$Q = (1 + R/R_q) \times [1/(2 + R/R_g)]$$

If $R = R_g$ is selected and $A = 1$, then $R_q = R/(3Q - 1)$

For the bandpass filter, the noninverting input should be used while leaving the inverting input open. The bandpass filter's center frequency, gain, and quality factor are:

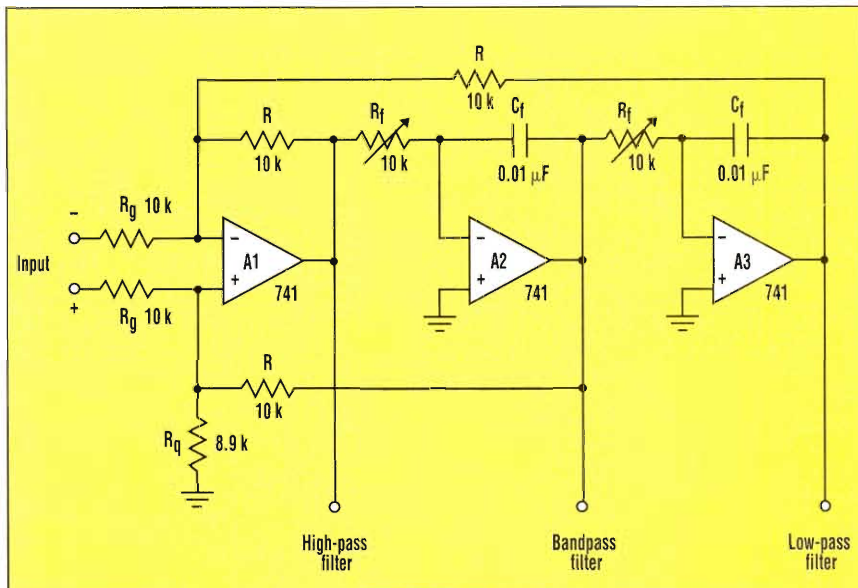
$$\omega_o = 1/(C_f R_f)$$

$$A = R/R_g$$

$$Q = 0.5[1 + (R/R_q) + (R/R_g)]$$

If $R = R_g$ and $A = 1$, then $R_q = R/[2(Q - 1)]$.

To have the bandpass filter's gain independent of the quality factor Q , the noninverting input should be used as the input. □



AMONG THE CHARACTERISTICS of this easily tunable state variable filter are its ability to simultaneously provide low-pass, high-pass, and bandpass filter functions, and that it can adjust bandwidth in a wide range by changing C_f and R_f values.

CIRCLE 521 CHECK FOR THERMAL RUNAWAY

JOHN DUNN

181 Marion Ave., Merrick, NY 11566.

Warning: Check your newly designed switch-mode power supplies for possible thermal runaway, which could occur hours, days, or even weeks later. And do so using a process that itself takes only a relatively short time. This is particularly important when the switching elements are power MOSFETs, whose on-resistance increases with rising temperature, a phenomenon that can easily lead to runaway.

Measure each MOSFET case temperature at regular time intervals from the moment power is applied. After the MOSFETs have reached an elevated temperature, turn the power off and continue to measure case temperatures at the same time intervals. The observed thermal time con-

stants during temperature rise and fall should be nearly equal. If not, it's almost certain that a thermal runaway condition exists.

The data sets in the GWBASIC program were taken at 10-second intervals on a 500-W MOSFET switch-mode supply (see the listing). For each data set, the program did a data-point plot, derived an exponential equation fitted to those data points, presented the exponential's thermal time constant "tau," and plotted the exponential equation itself for a visual comparison against actual data (see the figure). The user can compare the thermal time constants of temperature rise versus fall. Anyone can use this program by replacing the data shown with their own data.

With the MOSFETs mounted on

CIRCLE 522 LOW-COST STEP-DOWN REGULATOR

EUGENE E. MAYLE

R.L. Drake Co., 230 Industrial Dr., Franklin, OH 45005; (513) 746-4556.

An inexpensive and efficient discrete step-down voltage regulator can be built using a complementary transistor arrangement that uses both positive and negative feedback and is referenced to a Zener diode. A flyback conduction diode and a few passive components complete the circuit.

A general-purpose pnp audio output-stage transistor is chosen for Q1 (see the figure). In a common-emitter configuration, Q1 acts a "switch transistor" under the control of Q2, the "comparator transistor." The value of R_2 is chosen low enough to quickly discharge the parasitics of Q1 during turn-off, ensuring fast switching. R_5 is a precautionary element included as a base current-limiting mechanism for Q1. Q2, a general-purpose npn transistor, operates as a common-emitter in its positive-feedback mode and as a common-base amp in its negative-feedback mode. After initialization of power, bias resistor R_1 provides base current to turn on Q2, which turns on Q1. This results in additional bias current flow through network R_3 , R_4 , and C_2 . Thus, a positive-feedback loop is formed. Q1 and Q2 output currents ramp the voltage across C_3 . Zener diode CR2 eventually clamps the voltage at Q2's base while its emitter voltage at C_3 continues to rise. Once Q2's V_{be} drop becomes sufficiently small, Q2 turns off Q1, completing the negative-feedback loop.

The back EMF generated by L_1 forces Q1's collector negative, at which point it's clamped by Schottky diode CR1. The polarity of network R_3 , R_4 , and C_2 becomes reversed and shunts current away from Q2's base, enhancing the turn-off. A regulated bias point now is established at Q2's emitter and across C_3 . Regulation involves charging C_3 through L_1 , and the decay of C_3 through the load. If there's insufficient current draw from the load, R_3 will cause the out-

put to stabilize at about 0.7 V high. At light loads, charging time is almost load independent while decay is directly dependent. Overshoot can occur due to fixed circuit-response delays and ripple frequency will be low.

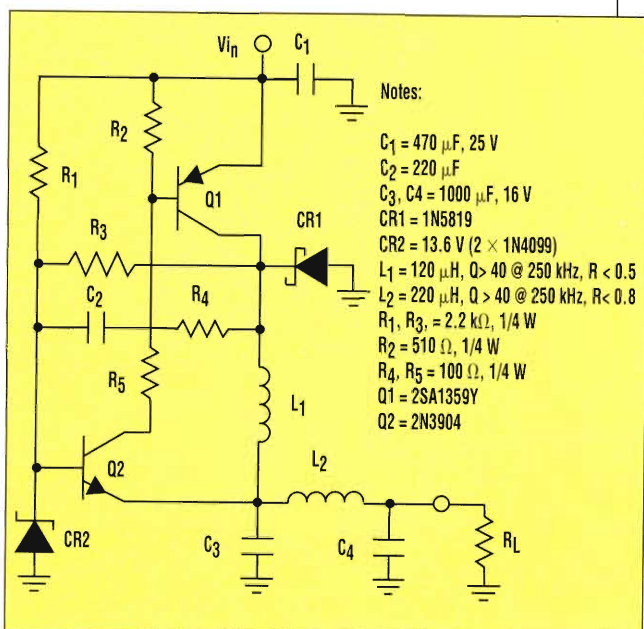
At higher loads, the charge-to-decay-time ratio approaches 1:1, the ripple voltage approaches a minimum, and the oscillation frequency peaks. Still heavier loads require that L_1 supply load current while charging C_3 , which increases the entire cycle—ripple frequency goes down and ripple voltage goes up.

Inductor L_1 is selected to maintain the switching frequency above the audible range for the intended operating load. The output filter L_2 and C_4 reduces ripple to less than 10 mV p-p over a large range of loads, with only a slight decrease in efficiency. □

Input = 18.0 V, Output taken at C3				
Output (V)	Load (Ohm)	Ripple		Eff. (%)
		(mVpp)	(kHz)	
12.54	1k	50	4	67
12.52	90.9	25	112	86.5
12.49	47.6	40	58	88.9
12.45	24.4	70	31	91.8

Input = 18.0 V, Output taken at C4				
Output (V)	Load (Ohm)	Ripple		Eff. (%)
		(mVpp)	(kHz)	
12.53	1k	58	.08	67
12.46	90.9	1.5	—	86.5
12.37	47.6	1.5	—	88.4
12.20	24.4	1.5	—	90.4

Output taken at C3, Load = 24.4 Ohms				
Input (V)	Output (V)	Ripple		Eff. (%)
		(mVPP)	(kHz)	
15.0	12.35	73	17.8	93.4
18.0	12.45	70	31.0	91.8
21.0	12.53	75	43.3	90.8



THIS inexpensive and efficient discrete step-down regulator is based on a complementary transistor arrangement that employs both positive and negative feedback and is referenced to a Zener diode.

CIRCLE 523 VERSATILE SLEW-RATE DETECTOR

CHUCK BAGG

17 Drake Rd., Fitchburg, MA 01429; (508) 342-7603.

This slew-rate detector, which can detect when a time-varying signal exceeds a certain rate of change, can serve in a number of useful applications (see

the figure).

For instance, as a pulse discriminator, it will respond to a fast-rising pulse, but will ignore a larger pulse that's too slow. With inputs of sine or

CIRCLE 521 BUILD A TWO-CHIP IF AGC NETWORK

ROBERT HOWALD

Martin Marietta Astro Space, P.O. Box 8555,
Philadelphia, PA 19101; (610) 354-3074.

A simple two-chip IF AGC circuit with wide dynamic range and excellent linearity can be achieved using Texas Instruments' TL026C voltage-controlled amplifier IC and a basic quad op amp, such as Linear Technology's low-noise LT1014. The circuit is attractive due to its simplicity and small size, while the TL026C's bandwidth make the device adaptable to signals with frequency ranges from video through low RF. Using a differential amplifier like the TL026C means that no coupling or splitting hardware is needed to realize the two paths for level control and output RF.

A diode detector, a low-noise dc gain stage, a reference-comparison amplifier/integrator, and a feedback difference network to the voltage-controlled device are among the functional components contained in the circuit. Because there are no tracking requirements and no AM information on the input signal, the integrator's time constant is very slow for this case.

The AGC circuit is designed to provide level control for a modulated,

constant amplitude signal in the 10-MHz range. As a result, the input is generally a static level, which may vary due to tolerances, gain variation, and signal-path differences between the originating source and the AGC loop. Slow level variations can be tracked, and the dynamics of the variations tolerated by the loop are a function of the loop's dominant time constant, which is governed by C_6 .

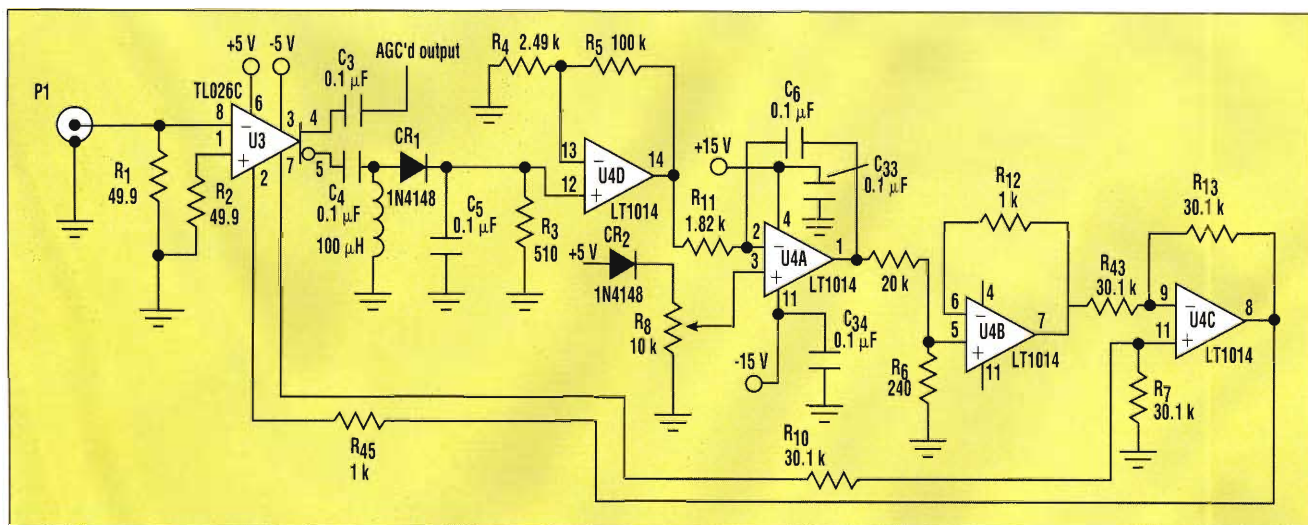
The AGC loop's ICs include the TL026C (U3), which is the differential variable-gain video amplifier; and the LT1014 (U4), which provides low-noise amplification of the detected output, comparison, and integrator stages, and includes the difference network that drives the AGC amplifier's control voltage (see the figure). Beginning at U3, the input comes in at P1, where it's impedance-matched. U3's dc power pins are 3 and 6, and the +5 V and -5 V are obtained by dropping down resistively or regulating the ± 15 V provided to the op amps. Pins 4 and 5 are the differential RF outputs. Pin 4 is directed to the following processing stages, while pin 5 feeds the AGC network for level control.

The load-driving capability of the TL026C is limited, so a relatively high-impedance next stage will conveniently avoid any problems if the signal level from the chip is high. In this device's case, it drove a high-speed op-amp summer, of which the input impedance is under the designer's control. Pins 2 and 7 of U3 are the control voltage pins. The output level is a function of the difference between these two pins (a negative gain versus voltage slope characteristic is described in the TI data sheets). The reference voltage of pin 7 is an output of the chip. The difference between the control voltage delivered to pin 2 and the pin-7 voltage controls the amplifier gain.

After U3 comes the detector circuit, which consists of L_1 , CR_1 , C_5 , and R_3 . As with any detector, L_1 and R_3 provide the dc current path to develop the dc voltage from CR_1 , which supplies the rectification to produce the dc component. Of course, C_5 provide the low-pass filtering action in conjunction with R_3 , and L_1 acts as an RF block while passing dc current.

The inherent low level of diode detection is boosted using the low-noise gain stage of U4D, which has a gain of about 32 dB. Higher voltage levels are more convenient to work with for comparison, particularly if a Zener or similar precision reference is applied directly.

The following stage is the integrator and comparator. The desired output level of U3 is set by adjusting the



A SIMPLE IF AGC CIRCUIT that features wide dynamic range and excellent linearity can be achieved with two chips: TI's TL026C voltage-controlled amplifier IC and Linear Technology's LT1014 (or any other similar) basic quad op amp.

R_3 potentiometer. Diode CR_2 tracks any temperature variation experienced by the detector diode (CR_1) to keep the output RF level constant over temperature variations. The U4A amp compares the reference to the detected voltage, which sets the desired output level. This controls the slewing of the integrator formed by R_{11} , C_6 , and U4A, so that it ramps in the proper direction. In steady state, of course, it's held constant from the feedback action. The integrator's output is delivered to the difference network.

The buffer amplifier, U4C, provides a high-impedance unity-gain amplifier following the voltage division of R_5 and R_6 . This attenuation assures that the transient voltage seen at the TL026C's voltage-control pin, while slewing toward the steady-state final value (such as at turn on),

doesn't exceed the IC's maximum allowable levels, where these absolute maximums reflect its ± 5 -V supply inputs.

Because the difference of U3's control pins determines output level, the reference voltage at pin 7 is summed at difference amplifier U4C. U4C subtracts the level-control voltage from the integrator's reference voltage. The reference voltage then is subtracted out by the comparison in the TL026C to determine gain level. This makes the output level independent of variation or drift of this reference. The feedback network is entirely under control of the external components, which can be selected for desired response. In addition, it simply makes the effective control voltage that derived by the network itself, which is easier to monitor, analyze, and troubleshoot externally.

The TL026C has nearly 38 dB of differential gain range, 36 dB minimum. For the single-ended output used in the circuit, the gain, as defined, is half of this, or 6 dB lower. About 23 dB was implemented, easily covering a maximum of less than 15 dB of dynamic range. The AGC amp's output was 360 mV p-p. In the middle 15-dB range of the AGC, with input power between -6 dBm and -21 dBm into 50 Ω , the measured output amplitude variation was typically 0.02 dB, with a maximum of 0.04 dB. Over the entire 23-dB range, the maximum change was 0.12 dB at the input power of -1 dBm. The operating point on the AGC-amplifier curve can be moved (centered) to meet more demanding input ranges. Also, as with any gain-controlled device, it can be cascaded to further extend the dynamic range. \square

CIRCLE 522 TUNABLE FILTERS COVER WIDE RANGE

RONALD MANCINI

Harris Semiconductor, P.O. Box 6883, MS58-096, Melbourne, FL 32902-0883.

An easily adjustable center frequency (f_c), symmetrical skirts, and an attenuation (gain) of -40(+40)dB at an octave on either side of the f_c is possi-

ble with the filter described here. The filter Q ($Q = f_c/BW_{3dB} \approx 250$) doesn't vary significantly when the center frequency changes. Consequently, the shape of skirts is essen-

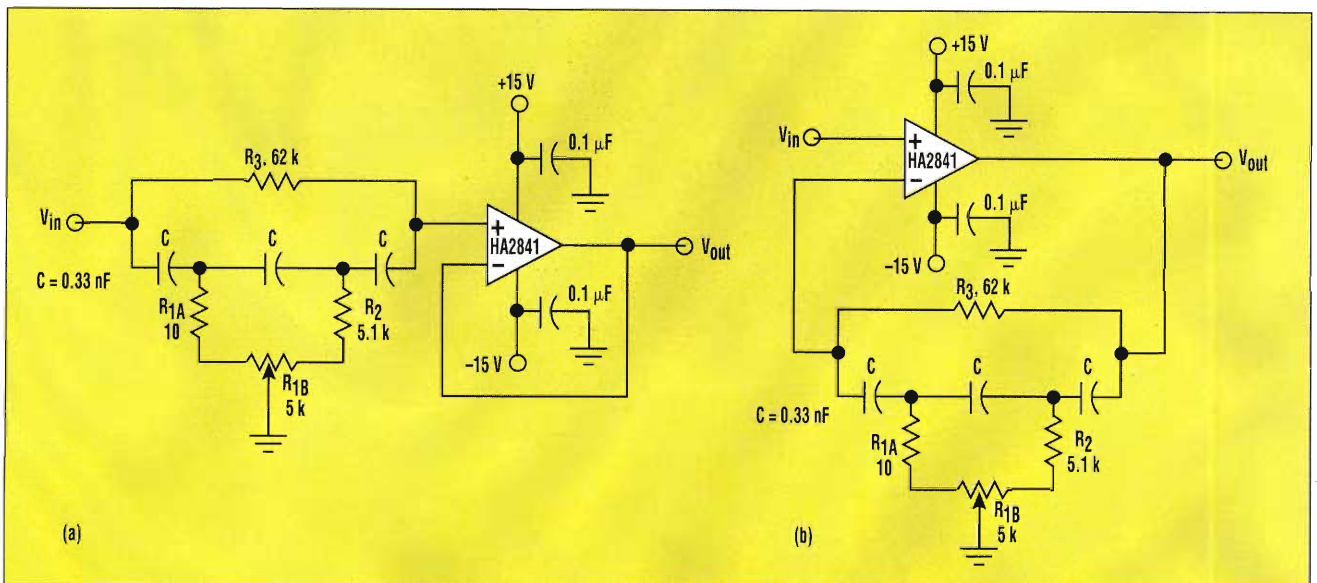
tially independent of the pot setting. Such a feature yields filters that can be adjusted over a much wider frequency range than "T" type filters, the only other type of filter with a deep notch or narrow bandpass. The calculation of the center frequency is given in equation 1; R_3 should be calculated with the aid of equation 2:

$$f_c = 1/[2\pi C(3R_1R_2)^{1/2}] \quad (1)$$

where $R_1 = R_{1A} + R_{1B}$;

$$R_3 = 6(R_1 + R_2) \quad (2)$$

A basic theorem of feedback cir-



1. THESE FILTER DESIGNS FOR bandreject (a) and bandpass (b) filters allow for easily adjustable center frequencies. The bandreject filter is passive, while the bandpass filter includes the passive network in the feedback loop.

CIRCLE 520 MULTIPLIER CAN SIMULATE A VCR

PAUL HENDRIKS

Analog Devices Inc., P.O. Box 9106, Norwood, MA 02062; (617) 461-3821.

A two- or four-quadrant multiplier with a summing input can be configured to simulate a resistor whose value is simply the ratio of a fixed resistor and control voltage (see the figure). Because the voltage-controlled resistor (VCR) topology possesses a well-defined transfer function, it may be more desirable than a JFET in some VCR applications. This VCR also can be used as a high-speed programmable dynamic load for applications in automatic test equipment.

The actual frequency response of the simulated resistor is determined by the bandwidth of the selected multiplier, the selected resistor val-

ue (R), and the control voltage (E_c). The AD835, a 250-MHz multiplier, which has a resistor value of 50 Ω , can simulate resistor values ranging from 50 to 3200 Ω with bandwidths of 10 MHz or greater.

The multiplier must have the general transfer function:

$$W = ((X_1 - X_2)(Y_1 - Y_2)/U) + 2$$

where the variables W , U , X , Y , and Z are all voltages. The denominator, U , is the scaling voltage while Z is the summing input. E_c , which may vary between 0 and U , drives the unipolar input of a two-quadrant multiplier or the highest distortion input (typically of the X input) of a four-quadrant multiplier.

The circuit's operation can be best understood by realizing that if the connection between Y_2 and Z is opened, the circuit would function as an inverted voltage-controlled current source, where:

$$I = (E_c/U)(V_{in}/R)$$

Incidentally, this circuit forms the

basis of a voltage-controlled integrator when it drives a capacitor, and can be used in the design of state-variable or biquad filters.

If the voltage-controlled current source is made to depend on an input voltage, V_{in} (i.e., by driving Y_2), as well as allowed to "float" on top of V_{in} (i.e., by connecting Y_2 to Z), then the input of Y_2 will simulate a resistor with the transfer function:

$$R_{in} = R(U/E_c)$$

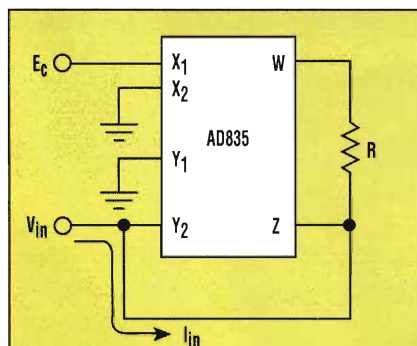
One node of the simulated resistor will always be referred to ground.

In practice, the characteristics of the simulated resistor will deviate from those of an ideal resistor due to the non-ideal characteristics of the multiplier.

For instance, the combined effects of both voltage offsets and input bias currents can be modeled as a dc voltage source in series with the simulated resistor (referred to analog ground).

Similarly, the total voltage noise seen at the output of the multiplier (W) can be modeled as a voltage noise source in series with the simulated resistor.

The effective input impedance of both the Y and Z terminals of the output will limit the maximum simulated resistance as well as interact with any series resistance connected to the multiplier's input (V_{in}). □



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} + Z$$

$$E_c = X_1 - X_2$$

$$W - Z = \frac{-E_c V_{in}}{U}$$

$$I_{in} = \frac{Z - W}{R} \text{ or } = \left(\frac{E_c}{U} \right) \left(\frac{V_{in}}{R} \right)$$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{\left(\frac{E_c}{U} \right) \left(\frac{V_{in}}{R} \right)} = \frac{R}{\left(\frac{E_c}{U} \right)}$$

$$R_{in} = R \left(\frac{U}{E_c} \right)$$

A TWO- OR FOUR-quadrant multiplier can be configured to simulate a resistor with a value that's the ratio of a fixed resistor and a control voltage.

CIRCLE 521 POSITIVE FEEDBACK TERMINATES CABLES

JERRY STEELE

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Positive feedback along with a series output resistor can provide a controlled output impedance from an op-amp circuit, with lower losses than would result from using an actual resistor. The circuit is useful occur when driving coaxial cables that must be terminated at each end in their characteristic impedance, which is often 50 Ω . Adding a 50- Ω series resistor on the op amp's output obviously reduces

the available signal swing.

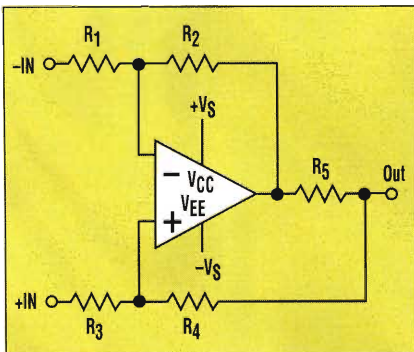
As can be seen in Figure 1, the circuit is an adaptation of the Improved Howland Current Pump, which is usually designed to maximize output impedance. It uses the positive feedback to provide a multiplication of the current sense resistor's value. For example, with $R_1 = R_2 = R_3 = 1$ k Ω , and $R_4 = 1.2$ k Ω , the circuit supplies a 50- Ω output impedance with only 5 Ω of real resistance to lose

voltage swing through.

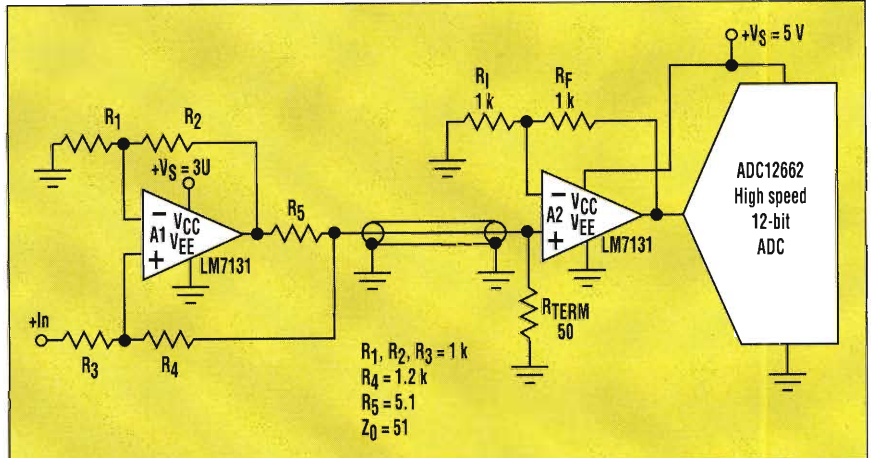
Adding positive feedback has the effect of multiplying circuit gain by the same ratio as it multiplies the sensing resistor (the example values given had a gain of about 10). Keep in mind that loading will cause the output voltage to drop to half (that's proof of the concept), so the loaded gain is half the unloaded gain. Available voltage swing remains essentially unimpaired. This can be a valuable feature, especially in low-voltage circuits like those used with National Semiconductor's LM7131. This part can provide 4-V pulses into a 150- Ω cable on 5-V supplies, but back termination would typically halve that. This technique maintains the full 4-V capability.

The circuit tolerates capacitive loads well, better than just the op amp alone. The inductive portion of any load is what could cause stability problems. Note that coax cable is a transmission line and isn't considered purely inductive or capacitive. Load inductance will manifest itself as overshoot in pulse response, if the overshoot is less than 40% of the total peak-to-peak amplitude of the pulse then the circuit has adequate phase margin.

Setting the desired gain involves pegging the values of the negative feedback resistors. Remember that the gain will ultimately be multiplied by an amount equal to what the series output resistor R_5 is being multiplied. For convenience, the input leg of the positive feedback (R_3) can be



1. COUPLING positive feedback with a series output resistor provides a controlled output impedance from an op amp circuit, reducing losses that would otherwise occur with an actual resistor. The circuit is an adaptation of the Improved Howland Current Pump.



2. THE VALUE OF THE TECHNIQUE demonstrated in Figure 1 is shown in this application, which uses National Semiconductor's LM7131 in a battery-operated piece of portable equipment operating at 3 V.

set equal to R_1 . The following equations solve for R_4 :

$$R_4 = \left[\frac{A_{ol}}{1 + A_{ol}(R_1/R_1 + R_2)} \cdot R_3 \right] \cdot \left[\frac{1 - R_5/Z}{Z} \right]$$

where Z is the desired output impedance. A_{ol} is the open-loop gain of the op amp.

An example demonstrates the value of this technique (Fig. 2). A1 is National's LM7131 in a battery-operated portable device operating at 3 V. At the 3-V supply, the LM7131 is specified for a maximum swing of 2 V. Using positive feedback for back termination makes this entire voltage swing available. At the receiving end, another LM7131 provides gain to present a 0-to-4-V input to a high-speed 12-bit ADC. □

CIRCLE 522 SIMPLIFY REMOTE GAIN CONTROL

DANA ROMERO

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Applications requiring remote control of gain can be simplified with the DS1666 digital audio resistor, from Dallas Semiconductor. One key advantage is that it can be used with or without a microprocessor/controller. The circuit requires only three ICs and a single 5-V supply to provide gain control via a PC printer port (see the figure, a).

U1 is connected as the feedback resistor for op amp U2, and R_2 is added to provide a complete loop when the resistance of U1 is zero. An ICL7660 power-converter IC (U3) is configured in the invert-only mode to supply -5 V from +5 V.

Part b of the figure illustrates the

input signal to U1 from the printer port. There are two important time delays: T_{CI} , which is the minimum between \overline{CS} going low and \overline{INC} going low; and T_{IL} , which is the minimum time that \overline{INC} should remain low to strobe the data from the U/\overline{D} signal.

If U/\overline{D} is high, the wiper will move toward the High end after an increment; if low, the wiper moves toward Low. Each increment advances the wiper once out of 128 positions, but the change in resistance is meant to resemble that of an audio taper potentiometer (increments are larger when the wiper is near the High end). Note that \overline{INC} is active on the high-to-low transition. In addition, the second \overline{INC} pulse is produced because

lator, use Equation 1 to calculate the value of frequency-setting resistors R_{F1} and R_{F2} :

$$R_{F1} = R_{F2} = 1 / (2 \times \pi \times 1 \text{ kHz} \times 10^{-9}) = 159.2 \text{ k}$$

Use Equation 2 to determine values for signal-magnitude-setting re-

sistors R_1/R_2 and R_3/R_4 :

$$R_1/R_2 = R_3/R_4 = [(V_O + V_{CC}) / (V_O - 0.15)] - 1$$

Assuming $V_{CC} = 15 \text{ V}$, then

$$R_1/R_2 = R_3/R_4 = 15.4$$

Setting R_1 and R_3 equal to 15.4 k and R_2 and R_4 equal to 1 k would pro-

vide the proper resistor ratios. These resistors act as loads to the internal op amp.

The maximum load current for the UAF42 is 10 mA (according to the suggested values given earlier, R_{fb} should be a 10-M Ω resistor). □

CIRCLE 522 IMPROVED CLIPPING CIRCUIT DESIGN

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This circuit is an enhanced version of the device described in "Clipping Circuit Has Precise Limits" (ELECTRONIC DESIGN, June 25, 1993, p. 69), which is built around a quad op amp

and an analog multiplexer (Fig. 1). It not only eliminates the analog multiplexer, but also increases the range of clipping levels.

Looking at its design, op amps A and D form unity-gain buffer ampli-

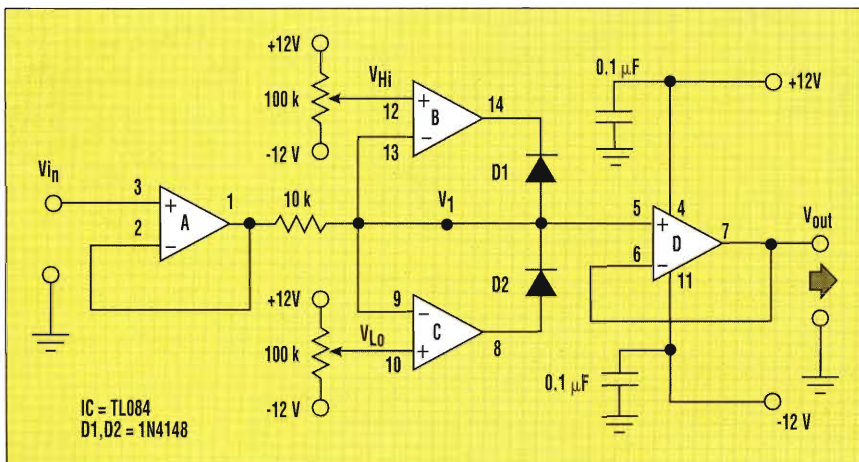
fiers. Op amps B and C compare the input voltage V_{in} with the reference voltages V_{Hi} and V_{Lo} . These references set the high and low clipping levels of the circuit.

When the input voltage lies in the range $(V_{Hi} - V_{Lo})$, the outputs of the comparators make both diodes D1 and D2 reverse-biased. As a result, the circuit's output V_{out} follows the input voltage.

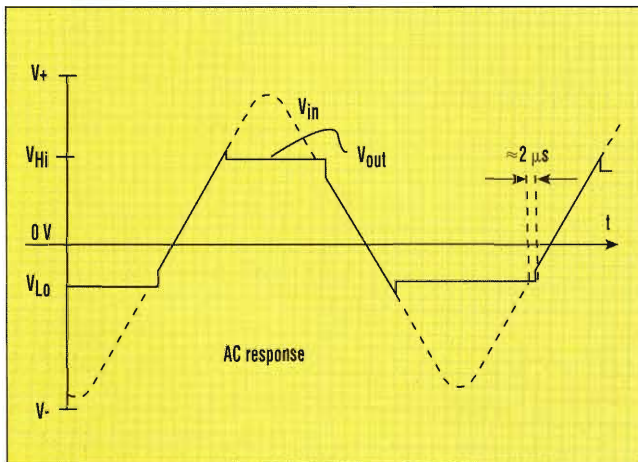
When the input voltage exceeds the value V_{Hi} , op amp B's output goes negative, forward-biasing D1 and, thus, reducing V_1 —the voltage at the inverting input of op amp B (Fig. 2). The circuit reaches an equilibrium condition at which $V_{out} = V_1 = V_{Hi}$.

Similarly, when the input voltage goes below the value V_{Lo} , op amp C's output goes positive, forward-biasing D2. This increases the voltage at V_1 . At the equilibrium condition, $V_{out} = V_1 = V_{Lo}$.

The circuit's output continues to follow the input for about 2 μs , even after the input voltage crosses the reference voltages, because of the slow rates of the op amps. The supplies ($5 \text{ V} \leq V_+ \leq 15 \text{ V}$, $-5 \text{ V} \geq V_- \geq -15 \text{ V}$) help energize the circuit. □



1. THIS CLIPPING CIRCUIT improves upon a previous Idea for Design submission (see the text) by eliminating the analog multiplexer. It also increases the range of clipping levels.



2. WHEN the input voltage exceeds V_{Hi} , op amp B's output goes negative, forward-biasing diode D1 and reducing V_1 . Similarly, when the input voltage goes below V_{Lo} , op amp C's output goes positive, forward-biasing D2.

CIRCLE 523 SAVE ENERGY IN SNUBBER NETWORK

FERNANDO GARCIA

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Leakage inductance, always a nuisance in switch-mode power supplies, is the main instigator of voltage overshoots. These voltage spikes may damage the power-switching devices unless tamed by a snubber network. Though snubber networks perform the required task of protecting costly devices, it comes at the expense of efficiency. The efficiency penalty is usually regarded as nominal, but with ever increasing requirements, additional techniques must be found.

One idea along that route would be to return the wasted snubber energy to an auxiliary output, such as, for instance, on flyback regulators. A flyback regulator offers the advantage of providing multiple output voltages with a single magnetic structure, and is therefore very compact and cost-effective (Fig. 1).

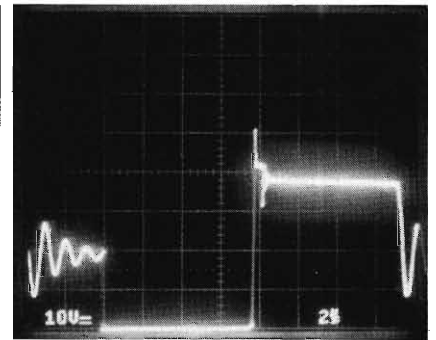
This particular circuit has a main

+5-V output and a +12.5-V auxiliary output.

The device being driven also required a "bias" voltage of +27 V with a few milliamperes of current. Originally, the voltage was going to be provided with a charge-pump technique, but closer inspection showed that the voltage could be obtained without any additional setup.

The heart of the regulator is formed by a National Semiconductor LM2577-ADJ "simple switcher" controller IC. The main and auxiliary voltage configurations came straight from the company's application literature, with resistors R_1 and R_2 providing the feedback for the main +5-V output. The auxiliary +12.5-V output is regulated by the intrinsic tight coupling of a discontinuous-mode flyback topology. R_3 and C_1 are compensation devices.

Whereas another winding could



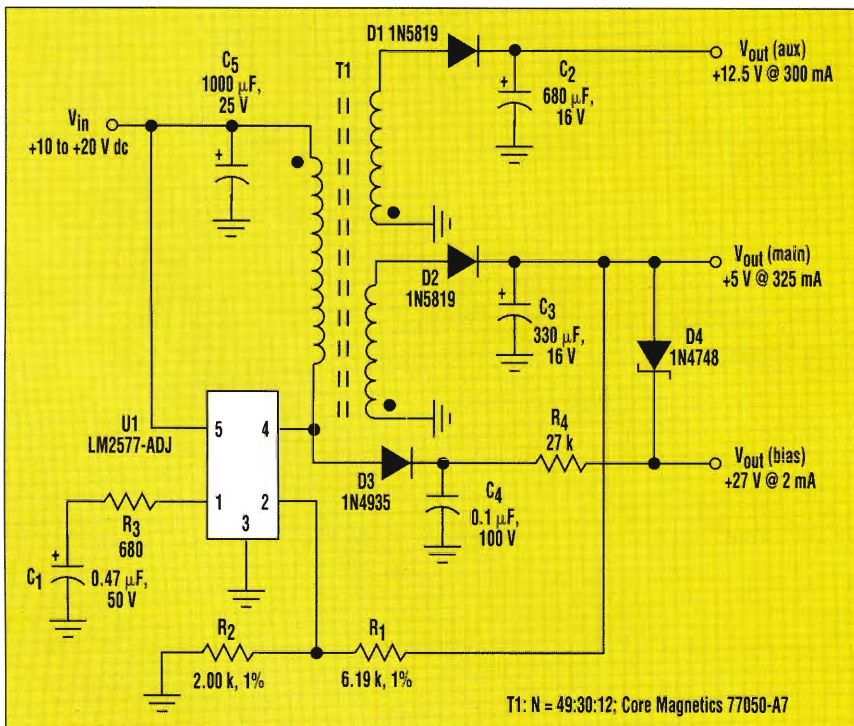
2. THE modified snubber network's operation at pin 4 of U1 is shown in this waveform (vertical scale: 10 V/div; horizontal: 2 μ s/div).

have been used in the transformer to provide the +27-V bias output, a "free" output may be realized from the voltage spikes in the primary winding being transferred via diode D3 to a reservoir capacitor (C_4). The charge in the capacitor is drawn by the current of both the bias load and the shunt Zener regulator D4. Enough charge is depleted from the capacitor to allow the next voltage spike to almost fully dump its energy in the next cycle.

In a sense, this is a modified snubber network where the energy is being put to good use instead of wasting it as heat on a resistor. Figure 2 shows the network's operation.

Further efficiency points may be gained by returning the shunt Zener current to the +5-V supply. The Zener current contribution is small enough to only negligibly effect the voltage regulation.

Because the capacitor doesn't discharge completely to 0 V due to the Zener's voltage, this modified snubber isn't as effective as the traditional "lossy" snubber. However, for applications that do not require extreme operating conditions, it offers a useful cost reduction and efficiency improvement. □



1. A FLYBACK regulator is a good application for implementing an energy-efficient snubber network. The network saves what would otherwise be wasted snubber energy by returning it to an auxiliary output.

CIRCLE 520 BIDIRECTIONAL ACTIVE LOAD

K.H. KANG

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When testing power supplies, power amplifiers, line drivers, and other circuits in which output current capability is a performance parameter, an active load that sinks or sources a constant current load is quite valuable.

Several years ago, Larry Carr presented an unidirectional active load circuit ("Dummy Load Keeps Current Constant," *ELECTRONIC DESIGN*, Oct. 1, 1992; p. 68.). It could only sink current from a unit under test (UUT). The design presented here is a single +9-V, battery-operated, bidirectional active load that can sink and source current (see the figure). This is a low-power design, consuming only about 140 μ A. The power MOSFET selected (IRF530 n-channel and IRF9530 p-channel), after derating, accepts a maximum load of ± 50 V at ± 5 A.

A bidirectional active load can be realized with a bipolar supply. For

single-supply design, a bipolar supply can be obtained with a dc-dc converter. This design, though, is a true single-supply circuit. The key to the design is to have two different sets of voltage levels at V_X , V_Y , and V_{SS1} : One set for current-sinking test, and the other for current-sourcing test.

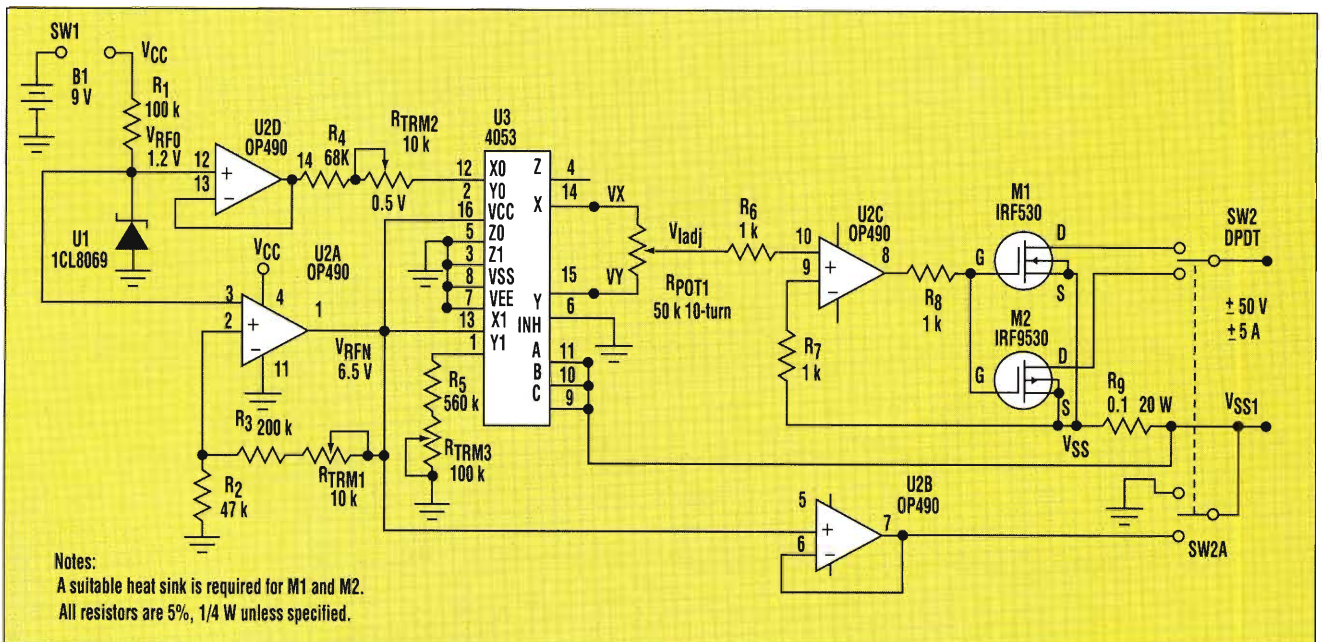
For UUT current-sourcing test, switch SW2 is set to the upper position, which connects the drain of MOSFET M1 to the UUT's positive terminal. Switch SW2A is ganged to SW2, therefore V_{SS1} is connected to the battery common. The required voltage levels for V_X and V_Y are derived from the 1.2-V voltage reference of U1 (ICL8069). The output of U1 is buffered by U2D, and drives a potential divider formed by R_4 , RTRM2, X0, X, RPOT1, Y, and Y0. Analog switches between X0 and X, and between Y and Y0, are turned on by a logic low at A and B of U3. The A and B signals are tied to V_{SS1} , which is already set low by switch SW2A.

By trimming RTRM2, V_X can be accurately set to 0.5 V. V_Y is switched to battery ground.

With the voltage levels of V_X and V_Y set, the voltage at the wiper of RPOT1 (V_{Iadj}) has a range of 0 to 0.5 V. Op amp U2C ensures that V_{SS} tracks V_{Iadj} . Consequently, $V_{Iadj} = I_D \times R_9$, which results in a load range of 0 to +5 A. The V_{DS} of MOSFET M1 is adjusted automatically to suit the UUT voltage, subject to a maximum of +50 V.

To test a UUT that sinks current at its positive terminal, SW2 is set to the lower position. This connects the drain of MOSFET M2 to the positive terminal of the UUT. SW2A then sets V_{SS1} to the level of V_{RFN} .

The voltage levels for V_X , V_Y , and V_{RFN} are set up as follows: U2A converts the 1.2-V reference to 6.5 V, which determines the voltage level of V_{RFN} . This is fed to a potential divider chain formed by X1, X, RPOT1, Y, Y1, R_5 , and RTRM3. Analog switches between X1 and X, and between Y and Y1, need to be turned on, which is done by pulling the A and B control signals high. These two high signals are provided by V_{SS1} , which is set to V_{RFN} . With such a potential divider chain, V_X can be trimmed accurately to 6.5 V (by using RTRM1), and V_Y to 6.0 V (by us-



THIS SINGLE-SUPPLY BIDIRECTIONAL ACTIVE LOAD CAN SINK and source current. The low-power design consumes only about 140 μ A. The key to the design is having two different sets of voltage levels at V_X , V_Y , and V_{SS1} . One set is for current-sinking test, while the other is for current-sourcing test.

ing RTRM3). This results in a voltage range of 6.0 to 6.5 V for V_{Iadj} . Feedback action by op amp U2C leads to $V_{Iadj} - V_{SS1} = V_{Iadj} - 6.5 V = I_D \times R_9$, to give a load range of 0 to $-5 A$. The $I_D \times R_9$ voltage is isolated from the UUT by M2, since V_{DS} of M2 is free to adjust to suit the UUT, subject to a maximum of $-50 V$.

V_X is trimmed to give 6.5 V to facilitate UUT current-sinking test; V_{RFN} is supposed to be at the same

level. There is, in fact, a slight difference due to the finite R_{on} of the analog switch from X1 to X_{on} —the specified resistance is 250 to 1300 Ω . The total resistance from X1 to Y1 and to ground is about 650 k Ω ; thus, the error is only about 1 in 650. Also, the U2B op-amp buffer isolates the circuit node of V_{RFN} so that the 6.5-V level won't be changed, due to external load impedance, when a UUT is connected for negative load test. □

distant targets. The preamplifier still must meet all of the other normal preamplifier criteria, such as bandwidth and noise performance. Moreover, the added time-dependent gain function must not degrade the signal.

This type variable-gain preamp can be built with a multiplier IC, the Harris Semiconductor HA2556. This IC establishes the signal bandwidth and noise figure because it's the only component in the signal path (see the figure).

The equation for the multiplier gain (as shown in the figure) is:

$$V_{out} = [V_X V_Y / 5] [(R_7 / R_8) + 1] \\ = 10 V_X V_Y$$

The HA5177 op amp and its associated circuitry make up a constant current source with a current, I , of $V_{D1} / R_2 = 51 \mu A$.

If switch S_1 is in the Linear position with Q2's gate held high, the current source is shorted to ground by Q2 and the multiplier gain is set to zero. When the transmission of the outgoing signal is complete, Q2's gate is brought low, forcing it into a very high drain resistance state (almost an open circuit). Consequently,

CIRCLE 521 BOOST ECHO-SYSTEM DYNAMIC RANGE

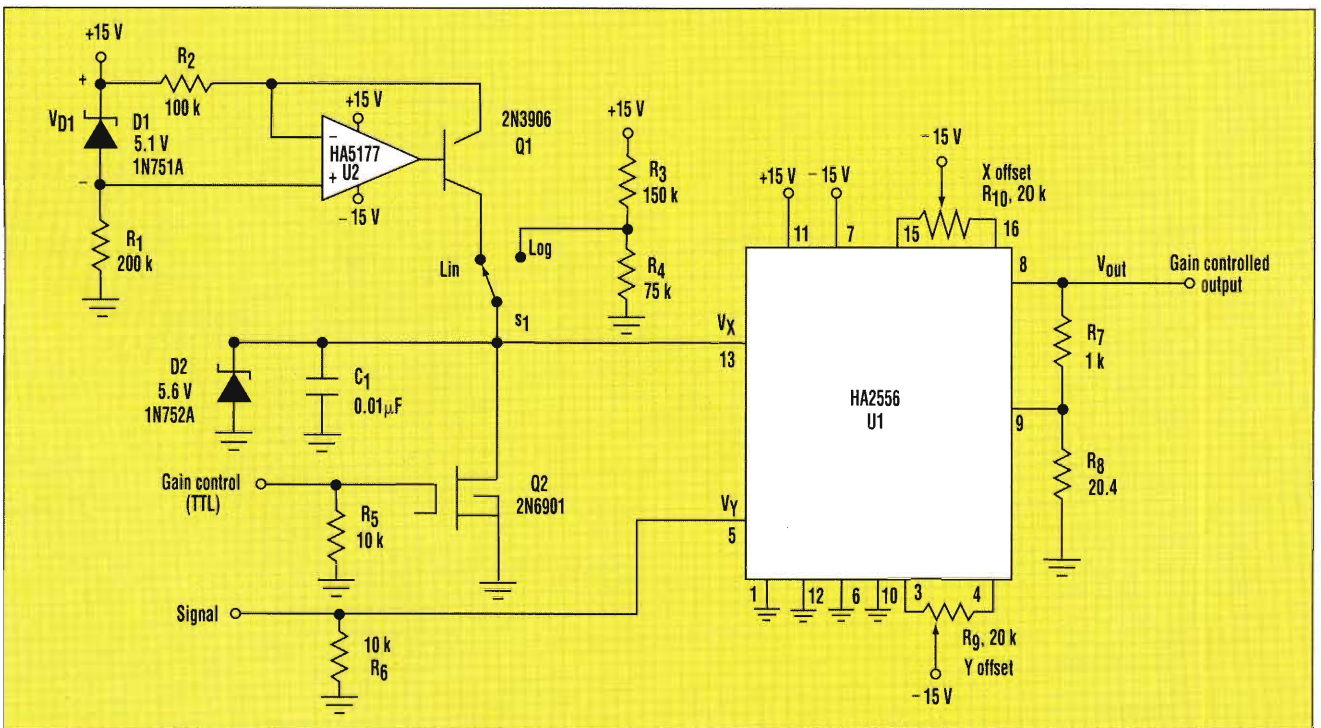
RONALD MANCINI

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32902-0883.

In an echo system, the returned signal amplitude is a function of the distance to the target, and it can be expressed mathematically as a function of time. An echo system with a fixed-gain preamplifier exhibits poor dynamic range because close targets (long return times) have high signal amplitudes while distant targets (long return times) produce amplitudes that are

much lower. In fixed-gain systems, the biggest signals establish the upper preamplifier gain limit based on not saturating the system. However, this gain may not be high enough to properly process the low-level return signals.

One solution involves a preamplifier that has a gain that is proportional to time, whereby the gain will be small for close targets and large for



USING A VARIABLE GAIN preamplifier helps improve the dynamic range of echo systems. Here, Harris Semiconductor's HA2556 multiplier is used to implement the variable gain preamplifier and establishes the signal bandwidth and noise figure.

IDEAS FOR DESIGN

the HA5177 current can charge C_1 in a linear manner.

The voltage across C_1 then ramps up from 0 to 5 V in 1 ms, which is the time it takes sound to travel approximately one foot through the air. During the first portion of the ramp, when the returned signal is very large, the multiplier gain is small because V_x is small.

As time increases, so does V_x , providing more gain through the multiplier as the expected echo decreases in amplitude. As a result, the output voltage swing of the multiplier tends to stay constant for large changes in input signal. In addition, the dynamic range is improved to the amount of

the ramp change, which is more than 60 dB with the values shown in the figure.

Because the returned signal often is a nonlinear function, linearizing it may be advantageous. An inverse nonlinear ramp can be employed to linearize the overall function. R_3 , R_4 , and C_1 generate a logarithmic ramp when s_1 is in the Log position, yielding a logarithmic gain function adequate for linearizing some transducers. Many other time-gain transfer functions can be generated by employing different types of ramps.

It's important to eliminate the multiplier offsets with the adjustments provided¹, because offsets

will appear in the output signal, reduce the dynamic range, and contribute errors. This circuit, as configured, will sweep from a gain of 0.01 as the ramp begins to 10 as the ramp ends. Returned signal amplitude is usually small, but shouldn't exceed 100 mV pp unless distortion can be tolerated.

The circuit's bandwidth can be as high as 57 MHz in low-gain applications, and is 5 MHz as configured. □

Reference:

1. "Wideband Four Quadrant Voltage Output Analog Multiplier Data Sheet," File Number 2477.3, Harris Semiconductor.

CIRCLE 522 OPTICALLY ISOLATED PRECISION RECTIFIER

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Isolation amplifiers and precision rectifiers are widely available functions. With this circuit, both functions can be combined in one topology (see the figure). It achieves excellent rectification symmetry and zero stability, and good linearity (better than 1%) and frequency response (> 10 kHz), with a minimum of precision components.

A1 acts as a voltage-to-current converter by servoing the current through the D1-D4 bridge and L_1 . Therefore, the voltage developed across R_1 equals the instantaneous input voltage. The diode bridge's full-wave rectification causes L_1 to be forward-biased regardless of the polarity of the input voltage. The magnitude of the bias controls the intensity of optical coupling between L_1 and Q1, and, thereby, the magnitude of Q1's collector current.

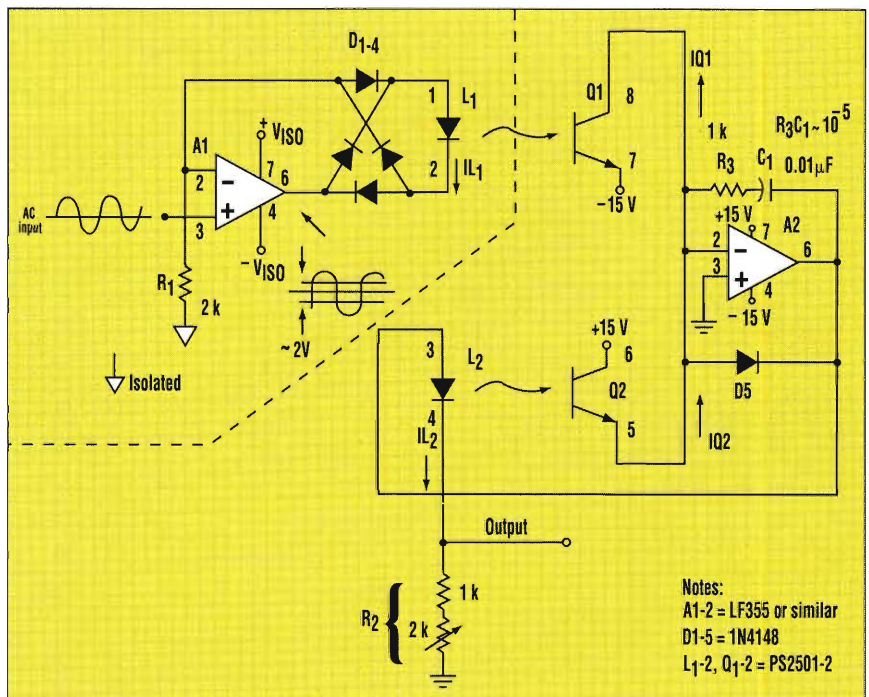
A2 servos the current through L_2 and R_2 so that the current passed by Q2 balances that passed by Q1. Because of the good tracking of elements of the PS2501-2 dual optoisolator, a constant ratio exists between L_1 and L_2 currents. Consequently, R_2 can be adjusted so that the output voltage across R_2 is equal to the rec-

tifier's isolated input voltage.

R_3 and C_1 provide frequency compensation for the L_2 -Q2 feedback loop. D5 prevents potentially de-

structive reverse bias of L_2 .

If the input voltage range is very large compared with the forward drops of D1-D5 and L_1 , such as when the 120 V ac mains must be monitored, A1 can be eliminated and the input voltage simply applied directly to the bridge, optoisolator, and suitable R_1 . All the while, good accuracy is maintained. Moreover, in this instance, the need for isolated dc power supplies for the isolated op amp would also disappear. □



Notes:
A1-2 = LF355 or similar
D1-5 = 1N4148
L1-2, Q1-2 = PS2501-2

AN ISOLATION AMPLIFIER and precision rectifier can be combined in one topology, as demonstrated here. Only a handful of precision components are required to attain its zero stability, better than 1% linearity, and excellent rectification symmetry.

CIRCLE 523 AUTOTRANSFORMER BOOSTS V_{OUT}

DANA W. DAVIS

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Step-up dc-dc converters that operate from small input voltages often possess correspondingly low maximum breakdown voltages of 5 to 6 V. This limits the maximum output voltage available from such devices. However, by adding an autotransformer, the output voltage V_{out} can be doubled without exceeding the IC's breakdown voltage.

A properly wound center-tapped inductor acts like a transformer with a 1:1 turns ratio. Combined with an

IC that typically boosts single-cell inputs as high as 6 V, it produces a regulated 9-V output with no more than 4.5 V across the IC (Fig. 1).

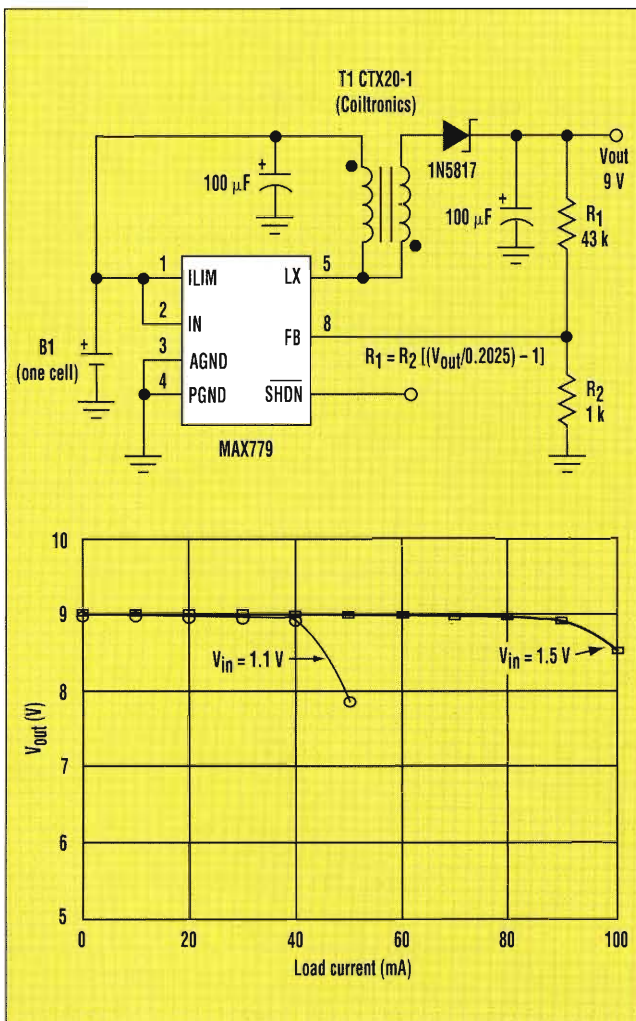
The circuit can be applied in smoke alarms as well as in other battery-operated equipment. It delivers an output of 30 mA at 9 V from a 1.1-V input, and as much as 90 mA at 9 V from a 1.5-V input.

A similar circuit setup for two-cell inputs delivers 30 mA at 9 V from 1.6 V, and a current of 80 mA at 9 V from 3.6 V (Fig. 2). □

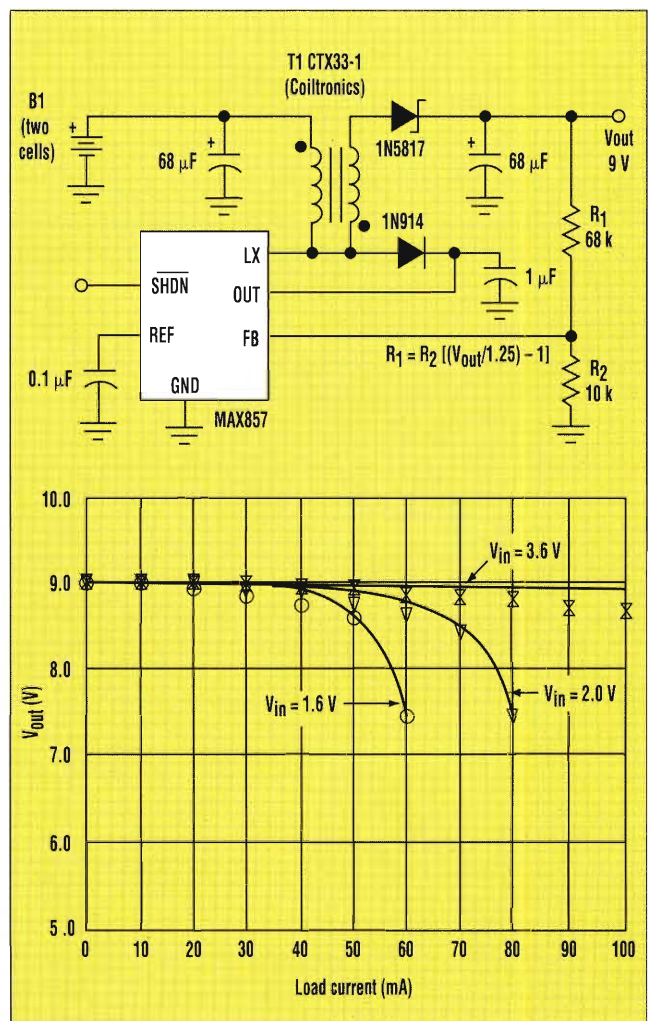
CORRECTION

There was an error in the equation in Jerry Steele's Idea for Design "Positive Feedback Terminates Cables," Mar. 6 issue, p. 92. The following is the correct equation:

$$R_4 = \frac{\left(\frac{A_{ol}}{1 + A_{ol}[R1 / (R1 + R2)]} \right) \cdot R_3}{1 - \frac{R_5}{Z}}$$



1. AN AUTOTRANSFORMER allows a low-voltage step-up converter to boost single-cell inputs as high as 10 V.



2. IN A SIMILAR SETUP to Figure 1, this circuit accepts two-cell inputs and generates regulated outputs as high as 10 V.

CIRCLE 520 FEEDBACK IMPROVES PEAK DETECTOR

TAMARA I. AHRENS

Elantec, 1996 Tarob Court, Milpitas, CA 95135; (408) 945-1323.

Diodes have long served as adequate rectifiers despite their large input voltages and low accuracy. The most common configuration for a simple diode peak detector (*Fig. 1a*) provides a mediocre 10% error for very large input voltages (*Fig. 1b*). If the diode is linearized, the necessary input voltage is only reduced to 1 V peak for the same 10% error.

However, the development of high-frequency op amps allows feedback circuitry to provide better accuracy and more sensitivity at the input. With feedback, peak detection is feasible at input voltages as small as 50 mV rms (*Fig. 2a*).

Looking more closely at Figure 2a, the input stage consists of a high-frequency op amp with an output that's into both a diode (D1), which functions similarly to the diode of a simple peak detector, and a clamping network, which limits the negative output swing of the forward op amp. The output of D1 is connected to the storage capacitor and is fed back to the input through a buffer. A storage capacitor of 0.1 μF is recommended for peak detection at audio frequencies.

A small resistance is shown in series with the storage capacitor to isolate it from the feedback loop. The smallest functional value is recommended for minimal peaking and maximum bandwidth; 10 Ω is suggested. A bleed current is necessary to allow the output to relax for a smaller input or in the absence of an input. In this case, 20 μA was chosen—it's small enough to avoid deteriorating the output value substantially, but large enough to dominate

the bias current of the feedback buffer.

The buffer's output is fed back to the negative input of the forward op amp through a resistor. This resistor buffers the emitter of the clamping network's pnp transistor from the low impedance at the buffer's output. Note that a compensation capacitor on the forward op amp may be necessary to ensure stability, and the output of the entire peak-detection circuit must be buffered to prevent a disturbance in performance.

The diode (D2) of the clamping network is always held on by the current source. For voltage signals greater than the peak held at the output, the

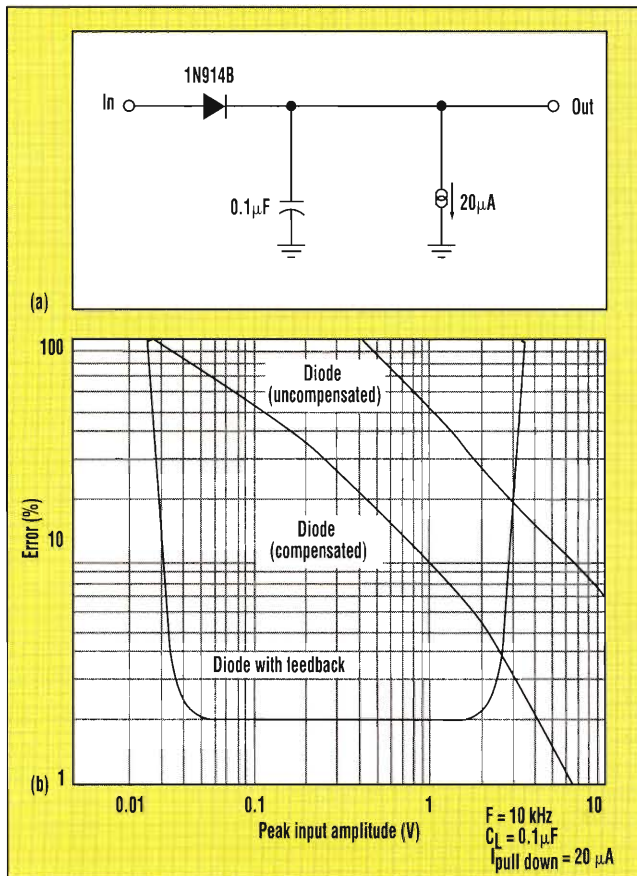
forward rectifying diode (D1) is conducting, and the output voltage is raised to match the input voltage. The buffer then feeds that voltage back around to the negative input of the forward op amp, and the emitter of the pnp transistor is held at the same voltage as its base, keeping it off and eliminating the second feedback loop.

For voltage signals less than the peak held at the output, diode D1 remains off. The pnp transistor's emitter is set as high as the output voltage by the buffer through the 1-k Ω resistor, while the transistor base is pulled down by the output of the forward op amp through the feedback diode (D2). The 270- Ω resistor adds a 0.3-V bias to the base of the transistor, producing a charge-discharge current ratio of 10,000:1. When the transistor turns on, a crude unity-gain feedback loop is completed through the clamping network (from the output voltage, down a diode

drop, and up the base-emitter diode of the transistor, to the input voltage) and a voltage drop builds across the 1-k Ω resistor. This clamping action minimizes the recovery time of the circuit.

Because the clamping network works like a unity-gain buffer for inputs less than the peak voltage, the output needs to slew less than one diode drop to turn on the rectifying diode (D1) for inputs greater than the peak voltage. In this manner, the clamping network prevents the forward op amp from exhibiting open-loop behavior and railing negative for inputs less than the peak voltage. This substantially reduces the slew rate necessary to achieve a desired bandwidth.

The circuit can function with amplitudes 30 times smaller than a simple diode peak detector. The EL2244 has an open-loop gain of 60 dB, raising smaller input signals enough to be detectable by the diode. The smallest recoverable amplitudes will be determined by the



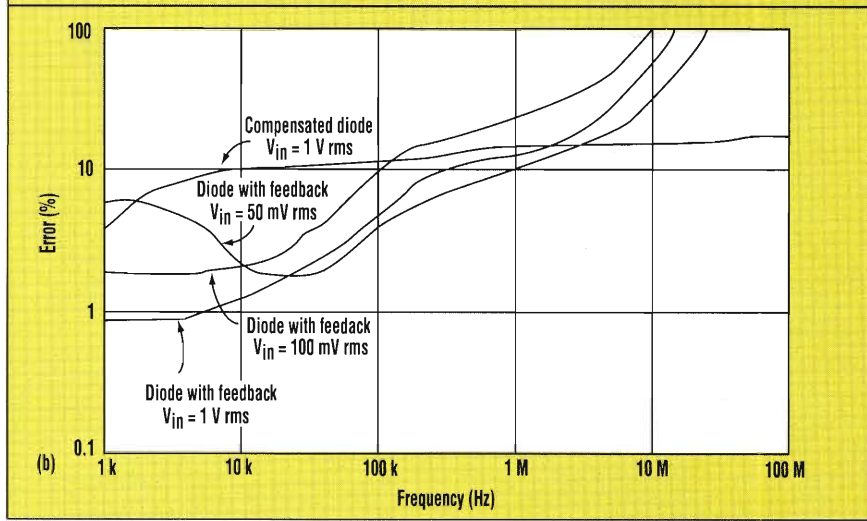
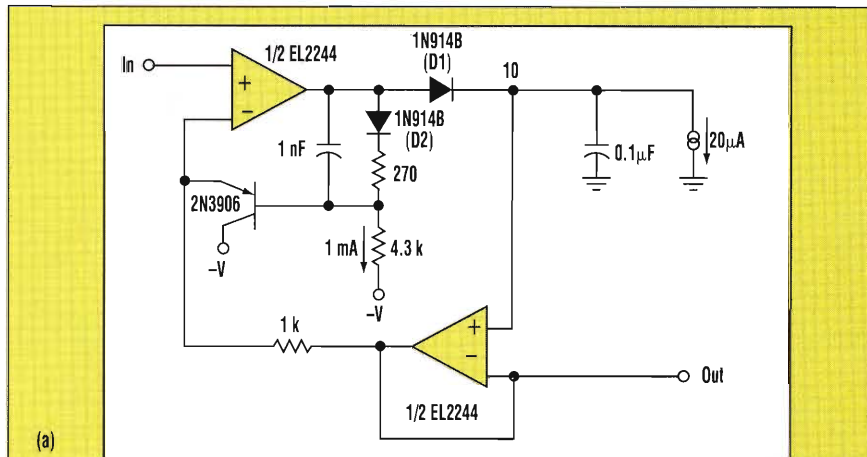
1. A SIMPLE PEAK DETECTOR, in its most common configuration, provides a mediocre 10% error for very large input voltages (a). If the diode is linearized, the necessary input voltage is only reduced to 1 V peak for the same 10% error (b).

noise amplified within the circuit. For the given circuit, this limit is approximately 30 mV rms input voltage. The largest allowable amplitudes will be determined by the input constraints of the op amp. For the EL2244 at ± 5 -V supplies, the maximum input range is approximately ± 3.5 V. If 5% errors are tolerable, this peak detector has a bandwidth of 100 kHz, making it ideal for audio applications (Fig. 2b). A considerable amount of small signal bandwidth and large slew rates are necessary to swing quickly through the dead zone at the output of the first op amp. However, such quantities limit circuit performance.

Consequently, for a handful of inexpensive parts, a drastic improvement can be made in a peak detector's performance compared to that of a simple diode. By utilizing modern, high-speed op amps, the feedback diode peak detector offers almost two decades of input voltage range improvement while maintaining functionality into the megahertz range. \square

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.



2. FEEDBACK CIRCUITRY can provide better accuracy and more sensitivity at the input. Feedback makes possible peak detection at input voltages as small as 50 mV rms (a). If 5% errors can be tolerated, the circuit has a bandwidth of 100 kHz (b).

CIRCLE 521 GENERATE FIR FILTER COEFFICIENTS

FRANK N. VITALJIC
514 13th St., Bellingham, WA 98225.

The `calc_coeffs()` function can calculate FIR filter coefficients $h(i)$ for low-pass, high-pass, bandpass, and band-reject filter types (see the listing). For an odd-valued filter length N , coefficient values having even-symmetry about the $h[(N-1)/2]$ coefficient (i.e., $h(i) = h(N-1-i)$) will exhibit linear phase. This makes the filter's time delay (T_d) independent of frequency. $T_d = (N-1)/2f_s$, where f_s is the sampling frequency in hertz. The first half of the coefficients, 0

through $(N-1)/2$, are stored in the `filter_coeffs(MAX)` array.

To reduce stopband ripple, a Ham-

ming window (`window_type = SINGL`) is applied as weighted factors to the filter coefficients. By applying the window a second time (`window_type = DUAL`), the stopband attenuation substantially improved at the price of broadening the transition region (see the figure).

All filter types and filter lengths above 15 exhibit excellent passband ripple of less than 0.1 dB with respect to unity gain. The low-pass characteristics illustrate both the broadening of the transition region and deep stopband attenuation (see the table).

The FIR filter gain $H(f)$ can be

Filter length (N)	f2/fs	
	f2+0.05	f2+0.1
31	-11 dB (-6)	-59 dB (-23)
41	-19 (-10)	-57 (-52)
61	-56 (-23)	-57 (-96)
81	-59 (-54)	-59 (-88)
101	-58 (-82)	-61 (-88)
127	-62 (-81)	-69 (-90)
() dual windowed		

```
#include <math.h> // FIR FILTER COEFFICIENTS PROGRAM

#define MAXLEN 127 // Maximum filter length
#define MAX ((MAXLEN+1)/2)
#define PI (4.0*atan(1.0)) // Define pi constant
#define LPF 1 // Enumerate filter types
#define HPF 2
#define BPF 3
#define BRF 4
#define SNGL 1 // Hamming window
#define DUAL 2 // Hamming window squared

void calc_coeffs( int filter_type, int filter_len, int window_type
double f1, double f2, double *filter_coeffs )
// Calculates FIR filter coefficients for the four filter types:
// Low Pass LPF, High Pass HPF, Band Pass BPF, and Band Reject BRF.
// The coefficients are stored in the filter_coeffs array.
{
int i, flag = 0;
double ham_coeffs[MAX], A, B, C, F1, F2;

// Clear filter_coeffs array
for( i = 0; i < MAX; i++ ) filter_coeffs[i] = 0.0;

// Calculate Hamming Window Coefficients
for( i = 0; i <= (filter_len-1)/2; i++ ) {
double arg;
arg = 2.0 * PI / (filter_len - 1);
ham_coeffs[i] = 0.54 - 0.46 * cos(arg * i);
if( window_type == DUAL ) ham_coeffs[i] *= ham_coeffs[i];
}

// Calculate filter coefficients and pass through window
if( filter_type == BRF ) { F1 = 0.0; F2 = f1; }
else { F1 = f1; F2 = f2; }
for( ; ) {
for( i = 0; i < (filter_len-1)/2; i++ ) {
A = sin(2.0 * PI * ((filter_len-1)/2 - i) * F1);
B = sin(2.0 * PI * ((filter_len-1)/2 - i) * F2);
C = PI * ((filter_len-1)/2 - i);
filter_coeffs[i] += ((B - A) / C) * ham_coeffs[i];
}
if( (filter_type == BRF) && (!flag) ) { flag = 1; F1 = f2; F2 = 0.5; }
else break;
}

// Calculate DC component value of coefficients
if( filter_type == LPF ) filter_coeffs[i] = 2.0 * f2;
if( filter_type == HPF ) filter_coeffs[i] = 2.0 * (0.5 - f1);
if( filter_type == BPF ) filter_coeffs[i] = 2.0 * (f2 - f1);
if( filter_type == BRF ) filter_coeffs[i] = 1.0 - 2.0 * (f2 - f1);
}
```

calculated as follows:

$$H(f) = h[(N-1)/2] + 2 \sum_{i=0}^{N-3} h(i) \cos \left[2\pi \left(\frac{N-1}{2} - i \right) f \right]$$

for $f = 0$ to 0.5 Hz

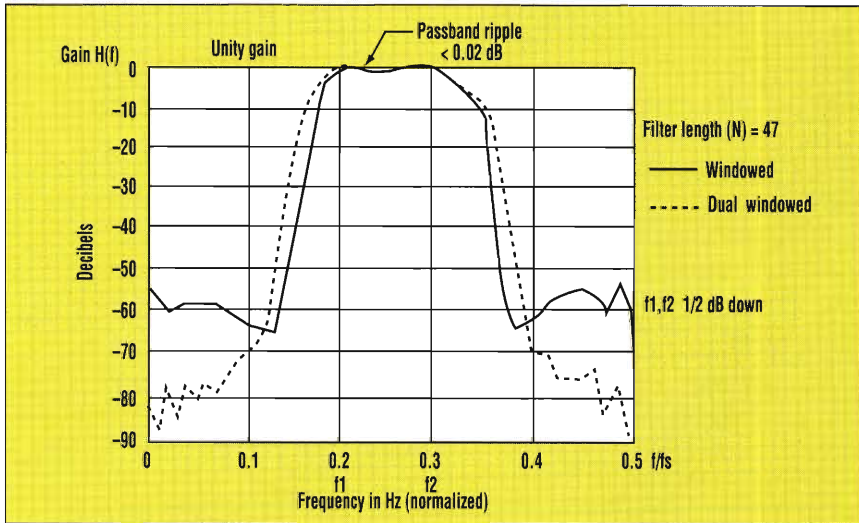
The f_1 and f_2 definitions (normalized) are:

Low-pass filter: $f_1 = 0$; $f_2 =$ cut-off frequency

High-pass filter: $f_1 =$ pass frequency; $f_2 = 0.5$

Bandpass/band-reject filter: $f_1 = f_{low}$; $f_2 = f_{high}$

At the pass frequencies, the gain is down 6 dB. A frequency offset (plus or minus) should be applied for other values of gain. □



THE CURVES show the FIR filter bandpass characteristic when applying a single Hamming window and a dual window. When the window was applied a second time, stopband attenuation improved substantially.

CIRCLE 522 SIMPLE ALL-PASS FILTER

EBERHARD BRUNNER

Analog Devices Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02602-9106; (617) 329-4700.

A very simple all-pass implementation can be realized with an active-feedback amplifier like the AD830 or the LTC1193 (Fig. 1). This article discusses circuit results using the AD830. R_1 and C set the filter's actual transfer function, while R_2 is needed to provide a purely real input impedance over the frequency range of the AD830 (necessary for measurement reasons).

The filter's two basic equations

are:

$$Z_{in}(s) = \frac{R_2}{2} \left(\frac{1 + sCR_1}{1 + s\frac{CR_2}{2}} \right)$$

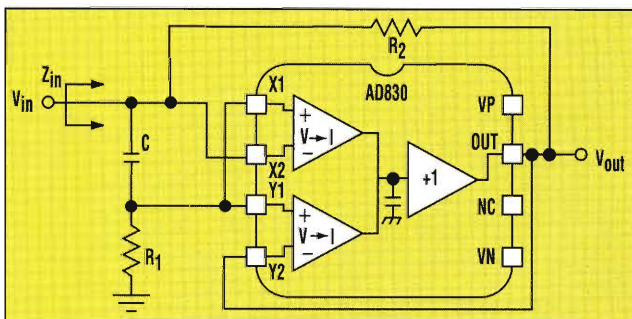
and

$$\frac{V_{out}(s)}{V_{in}} = -\frac{1 - sCR_1}{1 + sCR_1}$$

from which we can see that the magnitude is constant:

$$\left| \frac{V_{out}(\omega)}{V_{in}} \right| = 1$$

and the phase of



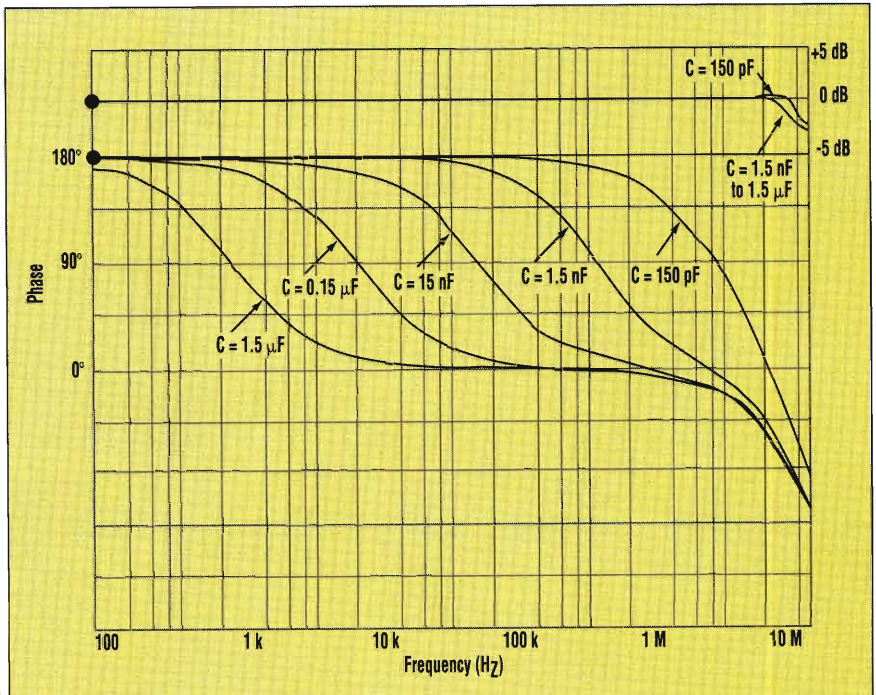
1. A SIMPLE ALL-PASS implementation can be created with an active feedback amplifier, such as the AD830.

V_{out}/V_{in} as a function of ω is:

$$180^\circ - 2 \tan^{-1}(\omega CR_1)$$

From Equation 1, it's clear that for Z_{in} to be purely real, R_1 has to be equal to $R_2/2$, which implies that $Z_{in}(\omega) = R_1$. In Figure 1, C was chosen to be 150 pF minimum to ensure that the input capacitance of the AD830 (2 pF) makes only a minor contribution. Once C is chosen, R_1 and R_2 can be picked according to the termination and required phase shift.

Figure 2 shows the circuit's performance for $V_s = \pm 15$ V, $R_1 = 100$, $R_2 = 200$, and values of C from 1.5 μ F to 150 pF with 90° phase shifts at one-decade increments up to 10 MHz. 10 MHz is the maximum achievable input frequency for accurate phase shift of 90° and unity gain. A 100- Ω termination resistor at the input provides a 50- Ω source resistance for the network analyzer used. Also, note that the amplitude is a constant 0 dB to about 20 MHz. □



2. MAGNITUDE AND PHASE responses of the all-pass filter in Figure 1 are illustrated. The maximum achievable input frequency for an accurate phase shift of 90° and unity gain is 10 MHz. Note that the amplitude is a constant 0 dB to about 20 MHz. □

CIRCLE 523 EXTRA-LONG-INTERVAL TIMER

RANDALL J. GRIFFIN

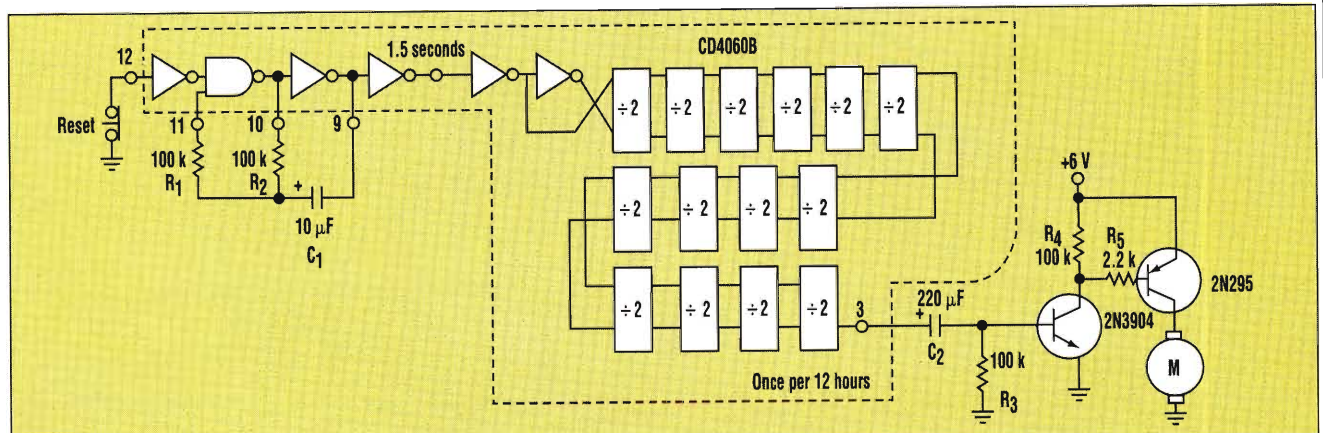
Norfolk Southern Corp., 312 W. Liddell St., Charlotte, NC 28206; (704) 378-3779.

This circuit came about when the need arose for an inexpensive timer that could pulse a motor or valve with a several-second burst once every 12 hours. One application would involve venting the condensation from a

compressed air tank.

The circuit is straightforward (see the figure). An RC oscillator consisting of R_1 , R_2 , and C_1 , with the internal gates on the CD4060, generates a 1.5-second clock that's subsequently divided to a 12-hour clock at the output.

Other times are available for output or for ANDing with the longer duration signals. The output is capacitively coupled to the two-transistor driver to provide a several-second pulse every 12 hours. The original supply was 6 V dc from a lantern battery, but it's governed only by the CMOS divider and the output transistors. The circuit can be configured many different ways. For instance, it could be used with a potentiometer to trim the input clock, or have it crystal-controlled over a wide frequency range. □



THIS INEXPENSIVE TIMER delivers a several-second pulse once every 12 hours.

CIRCLE
520

Read Back-EMF At Low Motor Speeds

JOHN PARRY and JEFF KOTOWSKI, Silicon Systems Inc., 138 New Mohawk Rd., Nevada City, CA 95959.

To save costs associated with Hall-effect sensors, many new brushless-motor control schemes use ICs that determine the rotor position by sensing the motor's back-EMF signals. In a unipolar configuration, the control chip synchronizes the three phases of drive currents by detecting the moments when each back-EMF signal rises just above, or falls just below, the motor supply voltage (V_{BATT}) (see the figure). These instances are known as zero crossings.

Shifting the back-EMF signals down from the motor supply voltage to levels that are within the control IC's operating voltage range is usually accomplished by placing resistor divider networks at each motor coil

and at the motor supply voltage. Resistor dividers, however, attenuate the back-EMF signals. This makes detecting the zero crossings difficult, especially at low motor speeds, at which the back EMF may be less than 500 mV p-p.

Rather than attenuating the motor signals, this circuit merely shifts the signals down to a reference level, V_{REF} .

The MOSFET M1, along with resistor R1 and npn transistor Q1, create a reference current I_1 that is equal to $(V_{BATT} - V_{REF})/R_1$.

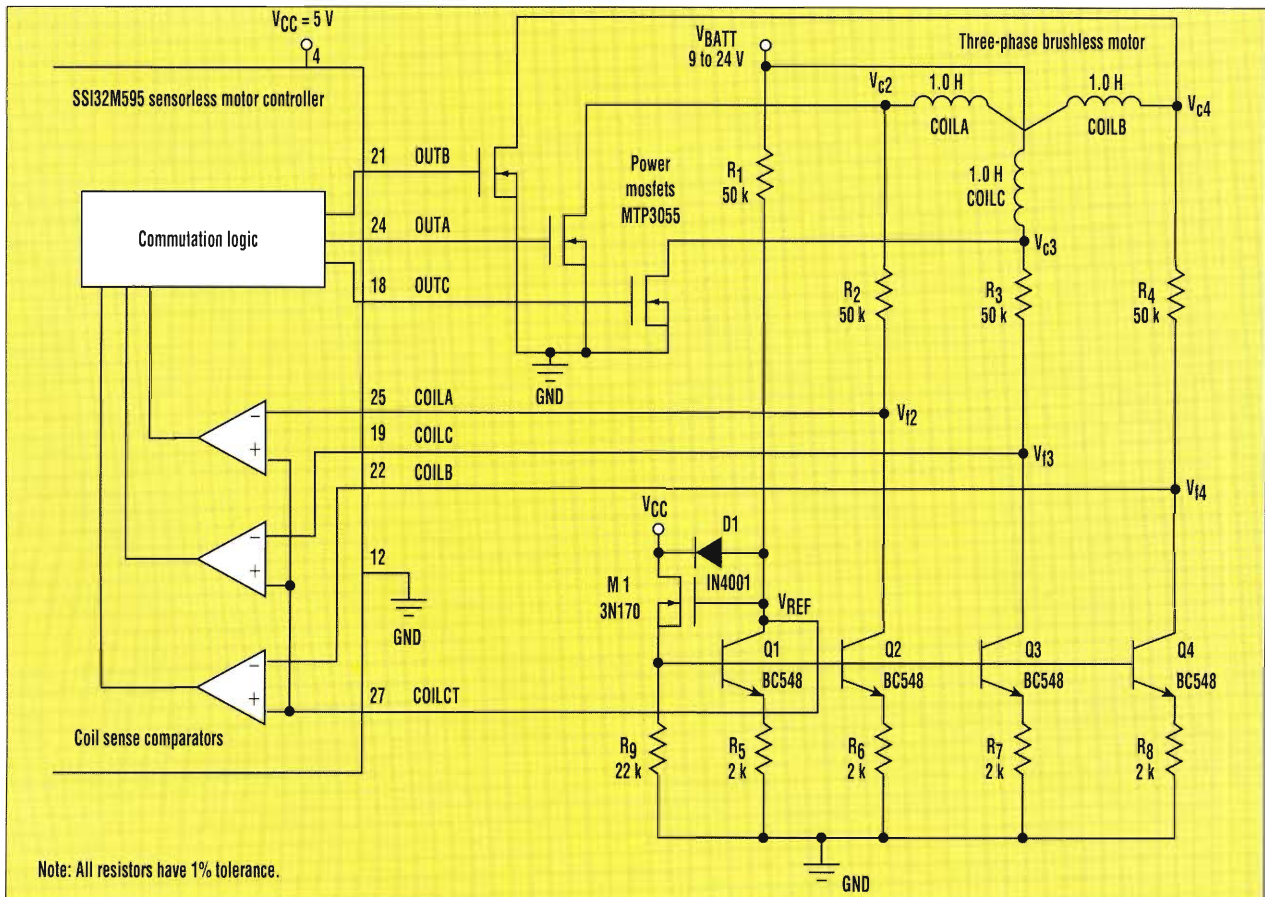
This reference current is replicated in Q2, Q3, and Q4. Because $R_2 = R_3 = R_4 = R_1$, the voltage drop across each resistor is the same. That means V_2 , V_3 , and V_4 vary above and below V_{REF} the same amount

as V_2 , V_3 , and V_4 vary above and below V_{BATT} .

Matching resistors R1 to R4 within 1% as well as R5 to R8 within 1% will resolve back-EMF signals as small as 200 mV. Diode D1 protects M1's gate from large transients on V_{BATT} . The ESD diodes on the SSI595, along with resistors R2, R3, and R4, protect the IC from damaging transients at V_2 , V_3 , and V_4 . □

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THIS UNIPOLAR CONFIGURATION CAN DETECT "zero crossings" simply by shifting the motor signals down to a reference level, rather than by attenuating the signals.

CIRCLE

521

Active Filter Uses Equal Value Parts

MICHAEL A. WYATT, Honeywell Inc., 13350 U.S. Hwy. 19, Clearwater, FL 34624; (813) 539-5653; fax (813) 539-2558.

Equal-value components can be quite an advantage in filter designs when considering the total costs associated with the procurement, stocking, and assembly of the filter.

For instance, the Butterworth active third-order low-pass filter (Fig. 1a, middle) uses equal value resistors and capacitors. This feature normalizes the filter's 3-dB corner frequency to $1/RC$ (in radians) for both low-pass and high-pass designs (Fig. 2a). The two additional op amps for the normalized filter may cost less than the unequal value components in the traditional Sallen-Key filter (quad op amps don't cost much more than single op amps), especially if the application calls for precision components (Fig. 1a, again).

PSpice's (MicroSim Corp., Irvine, Calif.) behavioral modeling capability allows for the comparison of the normalized and Sallen-Key third-order filters to an ideal filter. The Laplace behavioral voltage-controlled voltage source "EIdeal" (Fig. 1a, top) is configured as an ideal Butterworth low-pass filter with a 1-kHz bandwidth ($\omega_c = 6283.19$ radians/s). The Laplace transfer function (entered as symbol attribute of EIdeal) for the third-order Butterworth low-pass filter is:

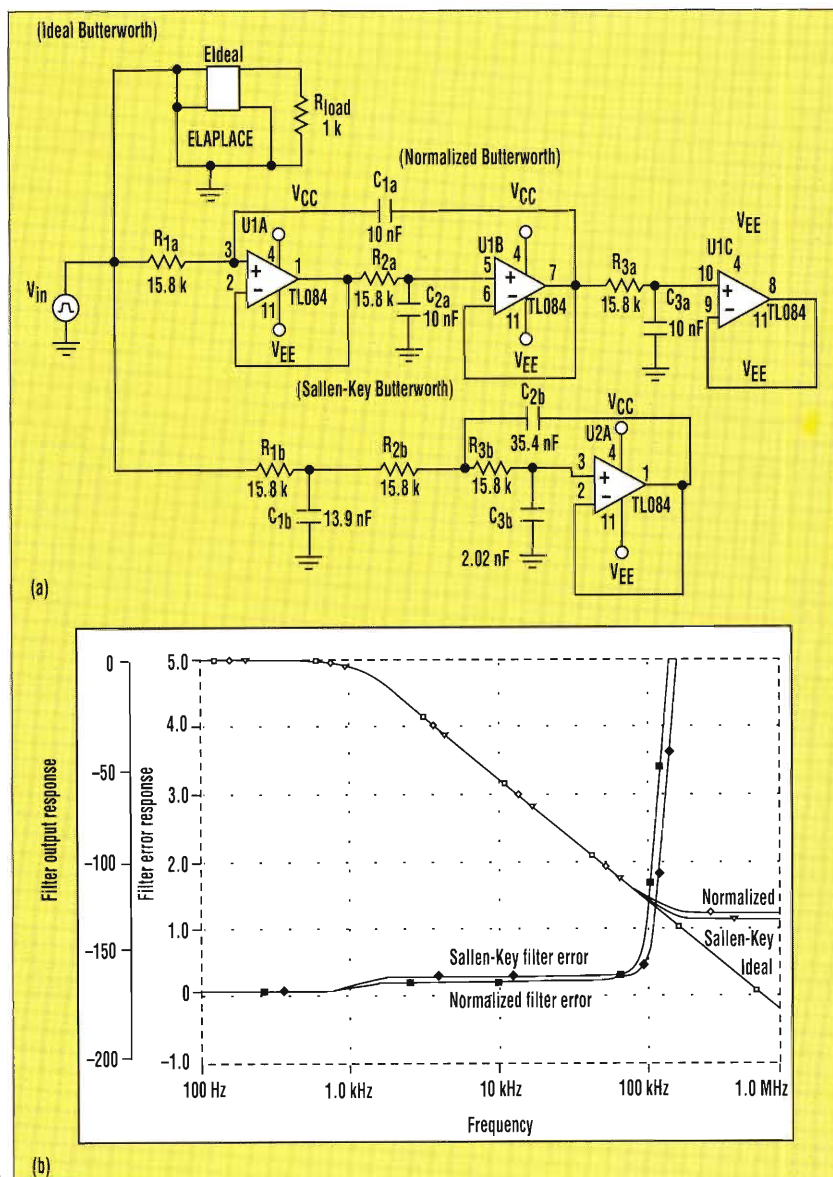
$$T(s) = \frac{1}{[(s^3 / \omega_c^3) + 2(s^2 / \omega_c^2) + 2(s / \omega_c) + 1]}$$

The graphs in Fig. 1b are plots of the ideal, normalized, and Sallen-Key low-pass filter frequency-domain magnitude and error responses. Note how both the normalized and Sallen-Key filters follow the ideal response well into the stopband. The error plots were created by plotting the dif-

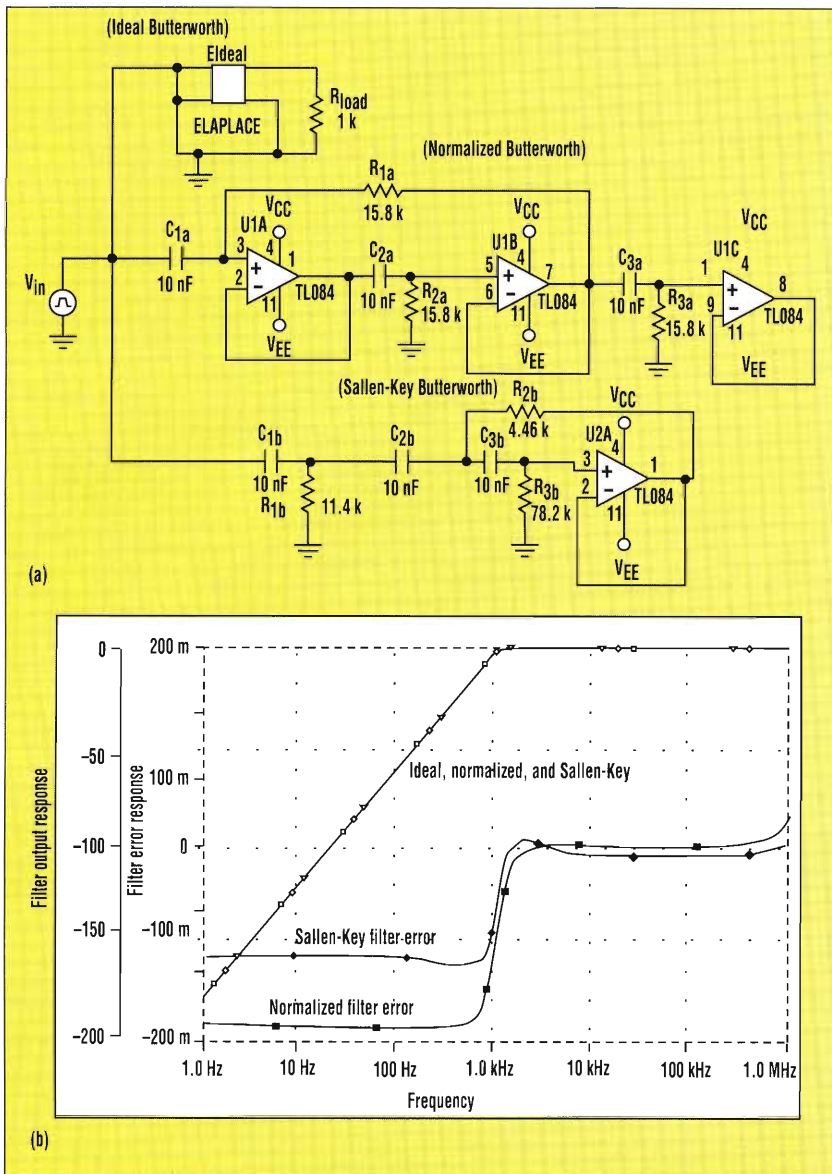
ference between the real and ideal filter responses.

The plots indicate that the normalized filter achieves performance results that are equal to those of the Sallen-Key low-pass filter.

Interchanging the resistors and capacitors transforms the normal-



1. USING EQUAL-VALUE COMPONENTS, in a third-order Butterworth low-pass filter design (a), will lead to lower total costs when procuring, stocking, and assembling the filters. Plots of the ideal, normalized, and Sallen-Key low-pass filter amplitude and error responses show that the normalized and Sallen-Key filters follow the ideal response well into the stopband (b).



ized low-pass filter into a high-pass filter with the same corner frequency (Fig. 2a). This concept is illustrated with an ideal Butterworth high-pass filter transfer function (EIdeal):

$$T(s) = \frac{s^3 / \omega_c^3}{[(s^3 / \omega_c^3) + 2(s^2 / \omega_c^2) + 2(s / \omega_c) + 1]}$$

Notice that the Sallen-Key filter must be modified according to impedance levels at each node. This yields a filter with equal-value capacitors and unequal-value resistors, an improvement over the traditional low-pass design of equal-value resistors and unequal-value capacitors.

The graphs in Fig. 2b indicate that the normalized high-pass filter compares favorably with the Sallen-Key filter in high-pass applications, much like the previously mentioned low-pass case. □

2. A HIGH-PASS THIRD-ORDER Butterworth filter with equal-value components can also be built (a). The normalized filter once again compares favorably with the Sallen-Key in high-pass applications (b).

CIRCLE 522

Catch Lost Cycles In 3-Phase Power

T.D. WINTERS, Vought Aircraft Co., Dallas, TX 75265; (214) 266-5206.

Recently, our Avionics Simulation Lab was given the task of monitoring 120-V, 400-Hz three-phase power to determine if there were missing cycles causing momentary loss of power to the equipment. The main target was our power generator, a fully solid-state switching power am-

plifier that takes three-phase, 60-Hz power and converts it to three-phase, 400-Hz power.

We had problems with the 400-Hz generator internally detecting a failure and shutting down. Using a memory scope, we caught the missing-cycle problem, which was extremely intermittent and varied from 1 to 5 cy-

cles of the 400-Hz ac waveform. Some of these events would occur prior to an automatic shutdown of the generator, while others would not result in an automatic shutdown.

A simple interface card was constructed (Fig. 1) with its optocoupler outputs connected to the printer port of a standard PC (optocouplers were

